IPC/COMPACT6-2A, -2AC
IPC/NETSBC-6A2, -6AC

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1.3	22.10.2013	R. Newbould	Description of the power fail function added

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1 Introduction

1.1. General Remarks

The content and presentation of this document has been carefully checked. No responsibility is accepted for any errors or omissions in the documentation.
Note that the documentation for the products is constantly revised and improved. The right to change this documentation at any time without notice is therefore reserved.
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CompactFlash	trademark of SanDisk Corporation
DiskOnChip	registered trademark of M-Systems LTD
PC/104	trademark of PC/104 Consortium
PCI/104	trademark of PC/104 Consortium
Geode	trademark of Advanced Micro Devices (AMD)
Windows CE	trademark of Microsoft Corporation
Windows XP Embedded	trademark of Microsoft Corporation

1.2. Contents of this Documentation

This document addresses to system integrators, programmers and instructed installation and maintenance personal working with the system. It provides all information needed to configure, setup and program the IPC/COMPACT6-2A and IPC/COMPACT6-2AC system.

1.3. Naming Conventions

The exact product identification is IPC/COMPACT6-2A and IPC/COMPACT6-2AC. Throughout this documentation the product is reference through it's marketing name "IPC/COMPACT6-ML".
The same applies to the integrated base board. The exact board identification is IPC/NETSBC-6A2 respectively IPC/NETSBC-6AC. Throughout this documentation it will be referenced as "NETSBC-6AC".

1.4. Additional Products and Documents

1.4.1. Hardware Products

In order to mount the IPC/COMPACT7-ML correctly there are four different mounting kits which have to be ordered separately:

- IPC/MKITCP-1B: for rear mounting (DOC/IPC_MKITCP-1BE)
- IPC/MKITCP-2A: for bottom mounting (DOC/IPC_MKITCP-2AE)
- IPC/MKITCP-2C: for bottom mounting (DOC/IPC_MKITCP-2CE)
- IPC/MKITCP-2E: DIN rail kit (DOC/IPC_MKITCP-2EE)
- IPC/MKWBDUSB9-1A: front panel with 1xDUB9 cutout

- IPC/MKWBDUSB9-2A: front panel with 2xDUB9 cutout

For further assistance and information please contact the manufacturer.

1.4.2. Software Products

The following software products are useful together with the NETSBC-6AC processor board:

- IPC/NETIPCFW-6A: Firmware for NETSBC-6AC boards (contact manufacturer)
- IPC/IOCOMSW-1A: Sample program code and utilities for x86 based PC/104 systems
- Operating Systems: check chapter 6.4 for a list of supported implementations.

1.5. Documents and References

1.5.1. Syslogic Documentation

The following documents are *required* for correct installation and operation of the IPC/COMPACT6-ML:

- DOC/NETIPCFW6-E: User Documentation for NETIPC Firmware (contact manufacturer)
- DOC/IPC_IOCOMSW-E: User Documentation for programming examples and utilities

1.5.2. Standards and Books

The following documents are *useful* for additional information about PC/104 and IEEE 996.1:

- PC/104 Specification Version 2.3
- PCI/104 Specification Version 1.0
- IEEE 996: IEEE standard document 'Personal Computer Bus Standard'
- IEEE 996.1: IEEE standard document 'Compact Embedded-PC Modules'

The PC/104 Specification may be downloaded from the Internet (see address below).

- PC/104 Consortium
  www.pc104.org

The IEEE standard documents may be ordered directly from the IEEE or any standards document distributor (see addresses below).

- IEEE Standards Department
  www.ieee.org

- 'ISA & EISA, Theory and Operation' by Edward Solari (Annabooks, San Diego), ISBN 0-929392-15-9
- 'PCI System Architecture' by Tom Shanley / Don Anderson (Mindshare, Inc.), ISBN 0-201-30974-2

1.5.3. Datasheets

- Datasheet AMD Geode LX800 microprocessor
  http://www.amd.com/us-

en/ConnectivitySolutions/ProductInformation/0,,50_2330_9863_13022%5E13073,00.html

- Datasheet AMD CS5536 companion chip
  http://www.amd.com/us-en/ConnectivitySolutions/ProductInformation/0,,50_2330_9863_13022%5E13054%5E13083,00.html
- Datasheet Intel 82551ER Fast Ethernet Controller
  http://www.intel.com/design/network/products/lan/docs/82551ER_docs.htm
- Datasheet Intel 82551IT Fast Ethernet Controller
  http://www.intel.com/design/network/products/lan/docs/82551it_docs.htm

1.6. Items delivered

- The IPC/COMPACT6-2A comes with an IPC/NETSBC-6A2 base board and an enclosure.
- The IPC/COMPACT6-2AC comes with an IPC/NETSBC-6AC base board and an enclosure.

1.7. Installation

The firmware configuration and download is described in the appropriate firmware documentation.

Important Note

Before applying power to the IPC/COMPACT6-ML system, the NETSBC-6AC board must be configured correctly and mounted.

1.8. Safety Recommendations and Warnings

The products are intended for measurement, control and communications applications in industrial environments. The products must be assembled and installed by specially trained people. The strict observation of the assembly and installation guidelines is mandatory.
The use of the products in systems in which life or health of persons is directly dependent (e.g. life support systems, patient monitoring systems, etc.) is not allowed.
The use of the products in potentially explosive atmospheres requires additional external protection circuitry which is not provided with the products.
In case of uncertainty or of believed errors in the documentation please immediately contact the manufacturer (address see chapter 10). Do not use or install the products if you are in doubt. In any case of misuse of the products, the user is solely liable for the consequences.

1.9. Electro-Static Discharge

Electronic boards are sensitive to Electro-Static Discharge (ESD). Please ensure that the product is handled with care and only in a ESD protected environment. Otherwise a proper operation is not garanteed and the warranty is not applicable.

1.10. Life Cycle Information

1.10.1. Transportation and Storage

During transportation and storage the products must be in their original packing. The original packing contains a box with antistatic and shock-absorbing material. It is recommended, to keep the original packing in case of return of the product to the factory for repair. Note that the packing is recyclable.

1.10.2. Operation

The operating environment must guarantee the environmental parameters (temperature, power supply, etc.) specified in the technical specification section of the product manuals.
The main functionality of the IPC system is defined by the application programs running on the processor board. The operating system and application programs are not part of the delivery by Syslogic but are defined, developed and tested by the customer or a system-integrator for each specific application. Refer to the respective documentation for more information.

1.10.3. Maintenance and Repair

The IPC system features error- and malfunction-detection circuitry. Diagnostic information gathered is transferred to the applications software where it can be used. In the rare case of a module hardware-failure or malfunction, the complete board should be exchanged. The faulty board must be returned to the factory for repair. Please use whenever possible the original packing for return of the product (ESD and mechanical protection).

1.10.4. Warranty

Our products are covered by a world-wide manufacturers warranty. The warranty period starts at the delivery time from our official distributor to the customer. The duration of the warranty period is specified in the respective product catalogs and the offers. All products carry a serial number for identification. The manufacturing data and deliveries are registered in a high level Quality Management System.
The warranty covers material and manufacturing defects. All products must be returned via the official distributor to the factory for repair or replacement. The warranty expires immediately if the products are damaged of operation outside of the specified recommended operating conditions. The warranty also expires if the date code or job number listed on the product is altered or rendered unintelligible. The warranty does not include damage due to errors in firmware or software delivered with the products.

1.10.5. RoHS

The products of the IPC/COMPACT6-ML family are designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC).

1.10.6. Disposal and WEEE

At the end of the life span the IPC products must be properly disposed. IPC products contain a multitude of elements and must be disposed like computer parts. Some of the IPC products contain batteries which should be properly disposed.

The products of the IPC/COMPACT6-ML are not designed ready for operation for the end-user and intended for consumer applications. Therefore the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable. But users should still dispose the product properly at the end of life.

2 Product Description

2.1. IPC/COMPACT-ML Systems

The IPC/COMPACT6-2A contains an enclosure and the IPC/NETSBC-6A2 motherboard. The IPC/COMPACT6-2AC contains an enclosure and the IPC/NETSBC-6AC motherboard. A list of main features of the motherboard can be found below:

2.2. Features of the IPC/NETSBC-6A2

CPU Core

- AMD Geode LX800 @ 0.9W low power industrial processor board eliminating the need for enforced cooling
- high performance 32-bit 8-stage pipeline x86 based processor core with efficient prefetch and branch prediction
- integrated Floating Point Unit (supports MMX and AMD 3Dnow! instruction sets
- 500MHz processor clock
- Split I/D L1 cache_64kB Instruction cache, 64kB Data cache
- Configurable L2 cache (I or D or both)
- 64-bit wide DDR SDRAM interface

Memory

- 512 Mbyte DRAM on board (DDR400, 200MHz)

Graphics Controller

- high performance 2D 64-bit graphics controller with backwards compatibility to VGA and SVGA standards
- CRT controller supporting up to 1920x1440x32 bpp at 85Hz and 1600x1200x32 bpp at 100Hz

CompactFlash and IDE Interface

- Enhanced IDE interface (ATA-5 specification) supporting 2 IDE devices with PIO modes 0 to 4, MDMA modes 0 to 2 or UDMA modes 0 to 5
- standard 44 pin IDE (2mm) connector for two external IDE devices
- CompactFlash Type I connector for onboard mountable CompactFlash card configurable as master or slave IDE device (replacing one of the external IDE devices)

Integrated Peripherals

- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- hardware watchdog configurable for 100 ms or 1.6 s timeout, hardware reset activation
- temperature supervisor for software controlled power management

PS/2 Mouse and Keyboard Interface

- PC/AT compatible keyboard controller (8242 compatible) with PS/2 mouse support
- Only available on an internal header

Serial Ports

- Six serial RS232 ports with 16 byte receive and transmit fifo (16550)
- COM2 and COM4 are optionally RS485
- COM5 and COM6 are 4 pin RS232 interfaces

Universal Serial Bus

- Four USB V2.0 ports (OHCI/EHCI-Host Controller)

Parallel Port

- standard PC/AT compatible parallel port
- IEEE 1284 termination network with integrated ESD protection
- standard PC/AT LPT1 address range
- usdes IRQ7
- available on an internal 2x13pin header

Ethernet

- Two 10/100baseT Ethernet interfaces

Firmware Flash Memory

- 16 MBit BootBlock Flash for BIOS, BIOS extensions and 1.44 Mbyte ROM-drive A: (floppy replacement), supporting easy firmware update through serial port

Add-On Memory

- 32 pin DIL socket for user installable Socket Memory supporting various types of 32 and 28 pin SRAM and EEPROM devices from 32 kbyte up to 512 kbyte
- battery backed through onboard battery or header

Real Time Clock

- Year 2000 compliant Real Time Clock (PC/AT compatible)
- battery backed through onboard battery or header

Configuration Switches

- Two rotary hex switches for customer application

Power Supply

- Onboard non-isolated power supply with wide input range (10Vdc … 30Vdc)
- Configurable power supply supervision (this function is only available on systems with revision 3 or higher)
- Monitors either external power supply voltage or it can be used as external power fail or on/off input (this function is available on systems with revision 3 or higher)
- Optional isolated power supply

2.3. Features of the IPC/NETSBC-6AC

CPU Core

- AMD Geode LX800 @ 0.9W low power industrial processor board eliminating the need for enforced cooling
- high performance 32-bit 8-stage pipeline x86 based processor core with efficient prefetch and branch prediction
- integrated Floating Point Unit (supports MMX and AMD 3Dnow! instruction sets
- 500MHz processor clock
- Split I/D L1 cache_64kB Instruction cache, 64kB Data cache
- Configurable L2 cache (I or D or both)
- 64-bit wide DDR SDRAM interface

Memory

- 512 Mbyte DRAM on board (DDR400, 200MHz)

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- hardware watchdog configurable for 100 ms or 1.6 s timeout, hardware reset activation
- temperature supervisor for software controlled power management

PS/2 Mouse and Keyboard Interface

- PC/AT compatible keyboard controller (8242 compatible) with PS/2 mouse support
- Only available on an internal header

CAN Interface

- Two SJA1000 stand-alone CAN controllre from NXP (Philips Semiconductor)
- BasicCan or PeliCAN mode
- supports CAN 2.0A protocol in BasicCAN mode
- supports CAN 2.0B protocol in BasicCAN mode (29 bit identifier accepted)
- sully supports CAN 2.0B protocol in PeliCAN mode
- 16MHz clock frequency
- configurable addressing mode (I/O or memory)
- configurable memory base address
- configurable for IRQ5, IRQ6, IRQ7, IRQ9, IRQ11 or IRQ15
- ISO 11898-24V compatible interface
- optical isolation (1000VDC)
- configurable termination resistor
- standard CAN-IN/CAN-OUT DSUB9 connector

Serial Ports

- Four serial RS232 ports with 16 byte receive and transmit fifo (16550)
- COM2 and COM4 are optionally RS485

Universal Serial Bus

- Four USB V2.0 ports (OHCI/EHCI-Host Controller)

Parallel Port

- standard PC/AT compatible parallel port
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- Onboard non-isolated power supply with wide input range (10Vdc … 30Vdc)
- Configurable power supply supervision
- Monitors either external power supply voltage or it can be used as external power fail or on/off input
- Optional isolated power supply

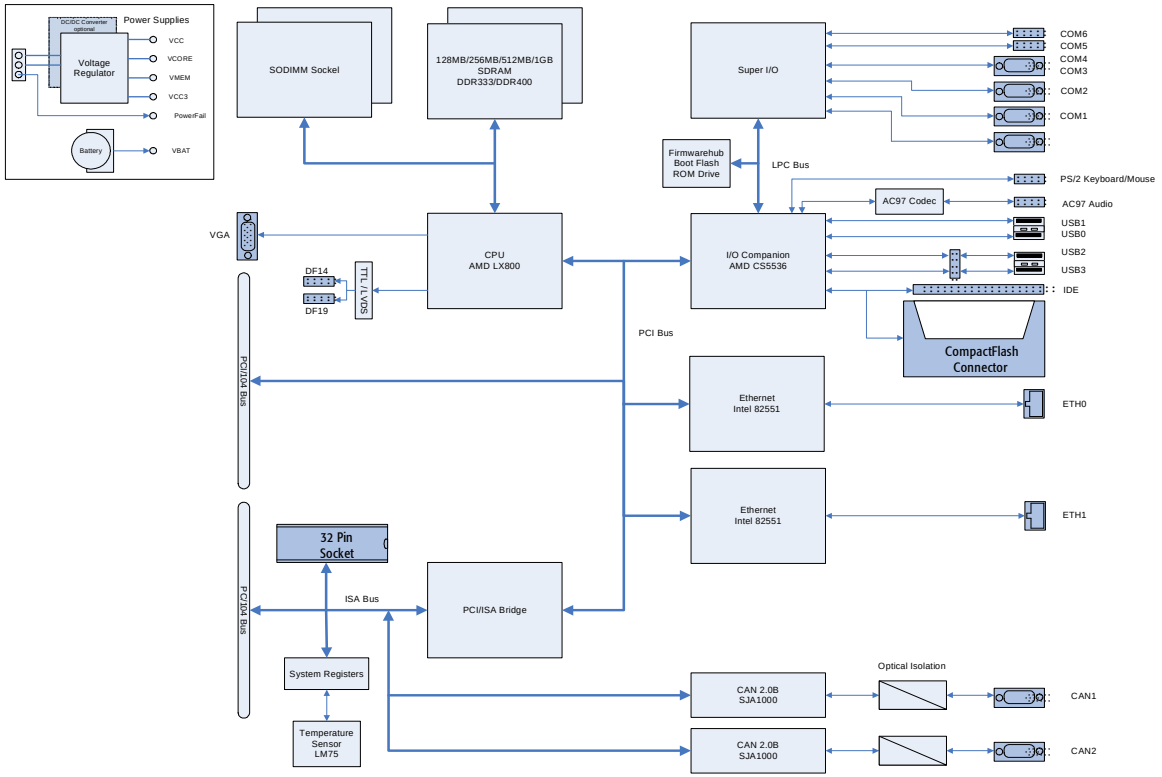

Fig. 1 Block Diagram (IPC/NETSBC-6AC)

2.4. Operating Modes

The IPC/COMPACT6-ML resp. NETSBC-6AC is based on the standard PC/AT architecture and therefore operates in DOS-compatible mode (real mode) on start up. The configurable BIOS initializes all onboard peripherals to their default values, executes the BIOS extensions programmed into the onboard Boot Block Flash by the user and BIOS extensions found on installed expansion boards prior to booting the operating system from a user-selectable drive (boot sector or OS image file). The operating system (or eventually a BIOS extension) may switch to protected mode to execute high performance 32-bit program code.

2.5. Startup Modes

The NETSBC-6AC doesn't support any special startup modes.

3 Hardware Description

3.1. Overview

The NETSBC-6AC board hardware may be configured by software (BIOS) and by jumper setting. Software configuration should always be done using the BIOS configuration program freely available as part of the NETSBC-6A firmware package IPC/NETIPCFW-6A, unless the BIOS does not support it (see firmware documentation DOC/NETIPCFW6 for details about supported BIOS configuration options).
The jumper and connector locations are shown in the board layout drawing (Fig. 3).

Important Note

Always check the jumper configuration of a freshly received board to comply with your system requirements before applying power, otherwise the system may get damaged or may fail to operate.

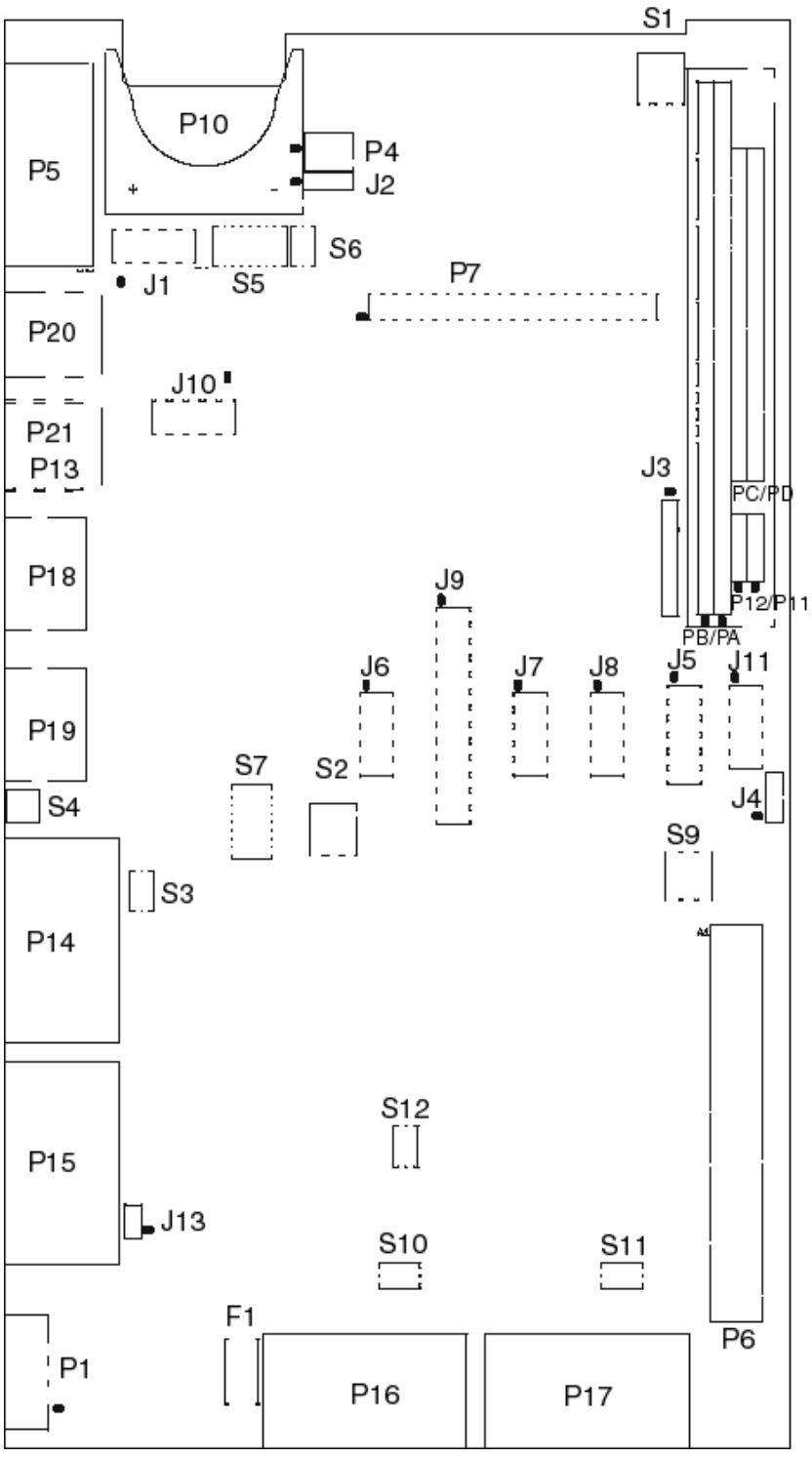

Fig. 2 Board Layout (NETSBC-6X)

3.2. Memory and I/O Resources

3.2.1. General Memory Layout and Configuration

The NETSBC-6AC uses the same memory layout as a standard desktop PC. Four onboard devices , DRAM, graphics controller, Boot Block Flash and Socket Memory, make use of the 4 GByte adressable memory space.

Address	Device / Register	Remarks
0000'0000..0009'FFFFh	640 kByte Main Memory (DRAM)	
000A'0000..000B'FFFFh	Video Memory	
000C'0000..000D'BFFFh	Configurable memory range (BIOS, BIOS Extensions, DRAM, Socket Memory or redirected to PC/104 bus)	see paragraph 3.7.1 and 4.2.3
000D'C000..000F'FFFFh	BIOS	do not write
0010'0000…01EAF'FFFFh	491 Mbyte Main Memory (DRAM)	free Memory above 1M
01EB0'000..01FAF'FFFFh	16MB Graphic Memory	do not access
01FB0'0000..01FFF'FFFFh	4MB SMM, Firmbase, VSA	do not access
8088'0000..83EF'FFFFh	Reserved	do not access
FFE0'0000..FFF7'FFFFh	1.44 Mbyte Firmware Flash	ROM drive
FFF8'0000..FFFF'FFFFh	BIOS/BIOS Extensions	do not access

Tab. 1 Physical Memory Address Space Layout

Important Note

The main memory above 1M isn't fully usable for applications. The main memory for applications is shared with the graphics memory (UMA: Unified Memory Architecture). The graphics memory can be configured from 4MB to 60MB. The default value is 16MB.
Firmbase and System Management Mode software and drivers for Geode's VSA (Virtual System Architecture) are located at the top of the extended memory range (e.g. 4MB). The graphic memory Size can configured in the BIOS. To calculate the remaining memory space the graphic memory size and 4MB of the Firmbase/SMM/VSA must be subtracted from the memory top.
IPC/NETSBC-6AC example: With the graphics memory size of 16 MByte (default), usable main memory ends at address:
- 01EAF'FFFFh (492 Mbyte free main memory)
This must be considered in operating system configuration (e.g. Windows CE).
Depending on Shadowing configuration the effective size may be slightly higher.

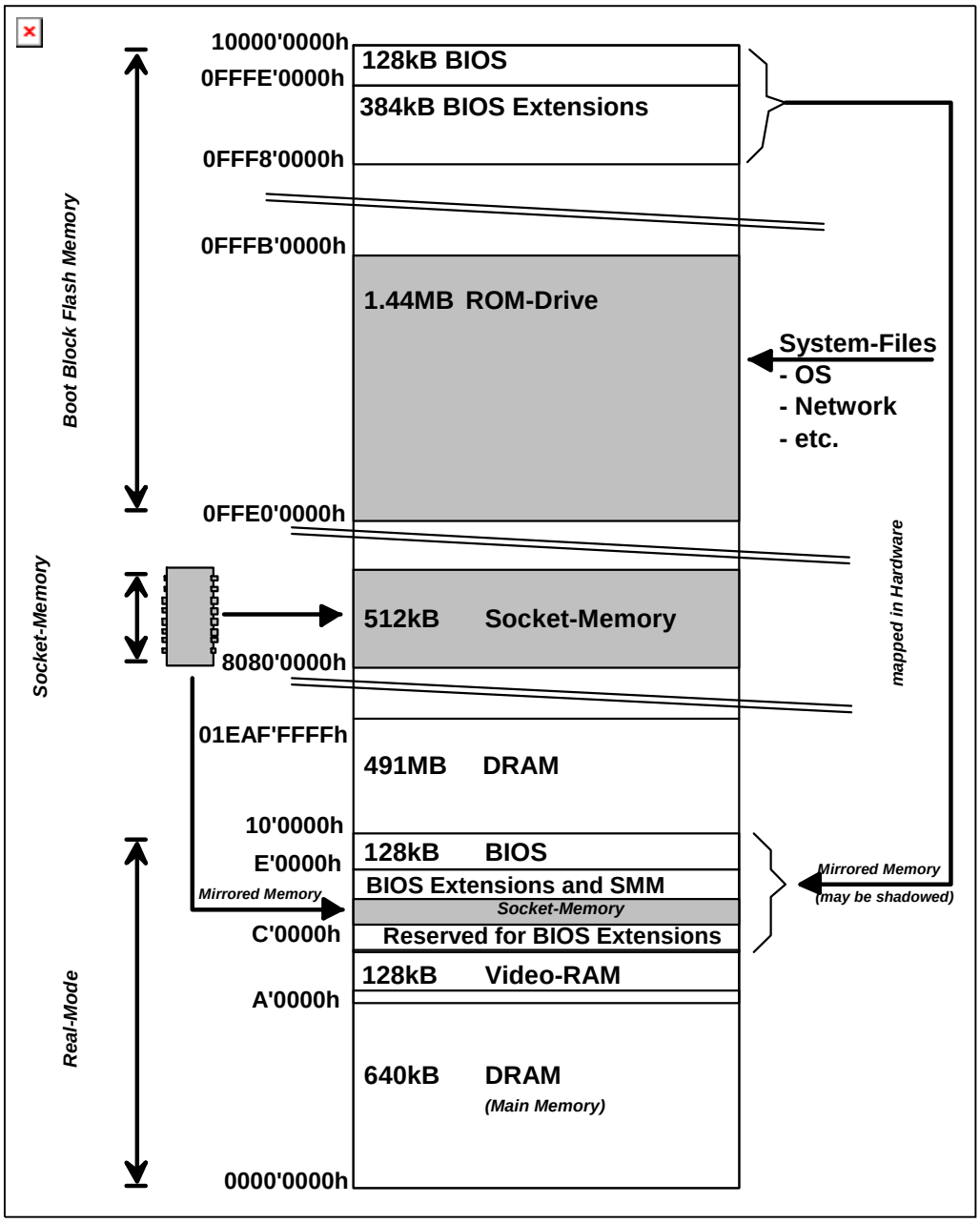

Fig. 3 Memory Map (IPC/NETSBC-6AC board)

3.2.2. General I/O Layout and Configuration

The NETSB's 64 kbyte I/O address space is mapped to the PC/104 bus address space as indicated in the table below. Note that 16 bit address decoding should be used on all PC/104 expansion boards to make efficient use of the I/O address space.

Address	Device / Register	Remarks
0000..000Fh	Slave DMA	
0020h	PIC Master – Command/Status	
0021h	PIC Master – Command/Status	
0040..0043h	PIT	
0060h	Keyboard/Mouse – Data Port	
0061h	Port B Control	
0064h	Keyboard/Mouse – Command/Status	
0070.0.071h	RTC RAM Addres/Data Port	
0072..0073h	High RTC RAM Address/Data Port	
0080h	Post Code Display	
0081..0083h	DMA Low Page	
0087h	DMALow Page	
0089..008Bh	DMA Low Page	
008Fh	DMA Low Page	
0092h	Port A	
00A0h	PIC Slave – Command/Status	
00A1h	PIC Slave – Command/Status	
00C0h	Master DMA	
00C2h	Master DMA	
00C4/00C6h	Master DMA	
00C8/00CA	Master DMA	
00CCh	Master DMA	
00CEh	Master DMA	
00D0h	Master DMA	
00D2h	Master DMA	
00D4h	Master DMA	
00D6h	Master DMA	
00D8h	Master DMA	
00DAh	Master DMA	
00DCh	Master DMA	
00DEh	Master DMA	
0200..023Fh	free	avail. on PC/104 bus
0278..027Fh	Reserved for LPT2	
02E0..02E7h	free	avail. on PC/104 bus
02A8..02AF	COM6	if available
02E8..02Efh	COM4	
02F8..02FFh	COM2	
0300..033Fh	free	avail. on PC/104 bus

0340..036Fh	free	
0370..0372h	Reserved for Floppy 2	
374..375h	Reserved for Floppy 2	
0377h	Reserved for Floppy 2	
0378..037Fh	Reserved for LPT1	
03A8..03AF	COM5	if available
03B0..03BBh	VGA Registers (MDA)	
03BC..03BFh	Reserved for LPT3	
03C0..03CFh	VGA registers (EGA)	
03D0..03DFh	VGA registers (CGA)	
03E0..03E7h	free	
3E8..03EFh	COM3	
03F0.0.3F2h	Reserved for Floppy 1	
03F4..03F5h	Reserved for Floppy 1	
03F6h..03F7h	Primary IDE Channel	
03F7h	Reserved for Floppy 1	
03F8..03FFh	COM1	
0481..0483h	DMA High Page	
0487h	DMA High Page	
0489..048Bh	DMA High Page	
048Fh	DMA High Page	
04D0h	PIC Level/Edge	
04D1h	PIC Level Edge	
0500..07FF	Runtime Registers Super I/O	
0A78h	Plug'n Play configuration port	
0CF8..0CFFh	PCI configuration registers	
7600..76FFh	CAN Channel 1	if enabled, or else avail. on PC/104 bus
7700..77FFh	CAN Channel 2	if enabled, or else avail. on PC/104 bus
8200..821Fh	NETSBC-6AC system registers	
8220..827Fh	free	avail. on PC/104 bus
0D000..0EFFFh	reserved for PCI devices (VGA, Ethernet, USB, IDE)	

Tab. 2 I/O Address Space Layout

Only the I/O addresses which are marked with “avail. On PC/104 bus” can be accessed on the aforementioned connector and be used for additional peripherals. The other unused I/O space can’t be accessed because these cycles are claimed by the integrated South Bridge and not by the PCI/ISA Bridge.

3.3. AMD Geode LX800 CPU

The AMD Geode LX processors are highly integrated x86 processors for embedded applications. The LX800 integrates the core microprocessor and the north bridge into one device.

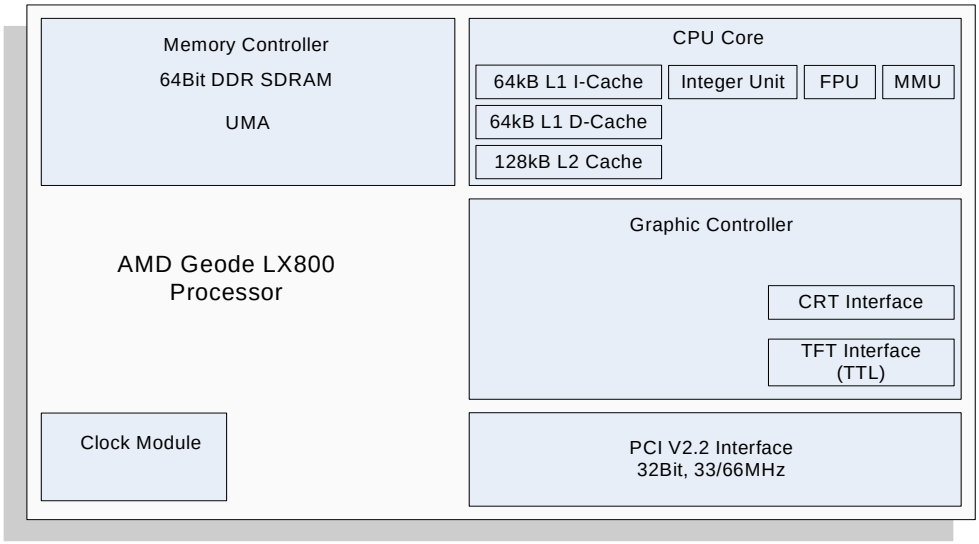

Fig. 4 AMD Geode LX800 processor

3.4. AMD CS5536 Companion Chip

The AMD Geode CS5536 companion device is designed to work with the LX800 microprocessor.

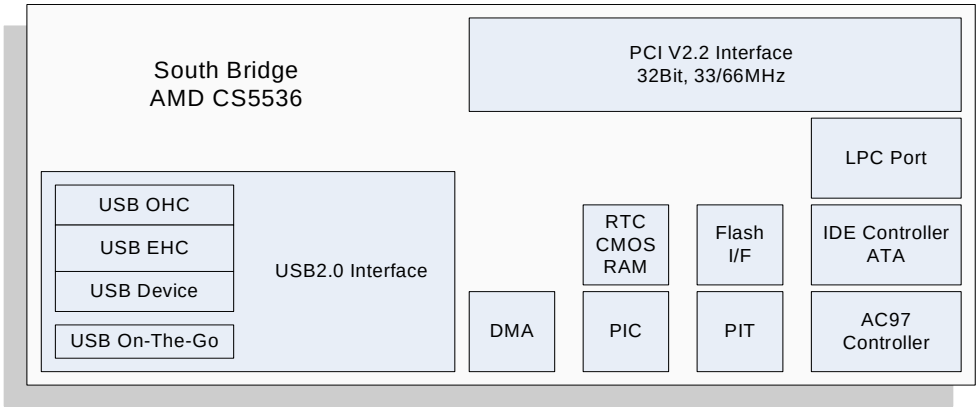

Fig. 5 AMD Geode CS5536 companion chip

3.5. PCI Devices

All devices follow the PCI 2.2 specification. The BIOS (and/or OS) control memory and I/O resources.

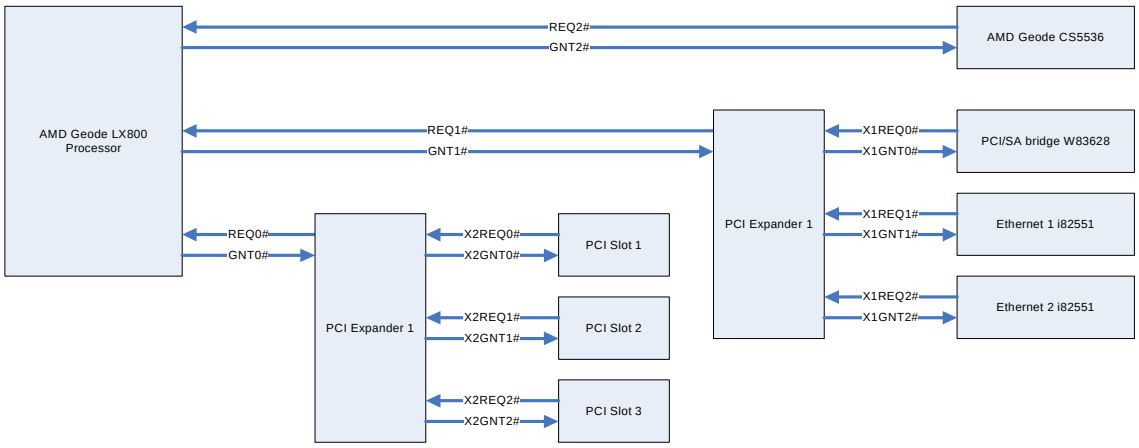

Fig. 6 PCI System

PCI Device (IDSEL)	Device ID	PCI IRQ	REQ / GNT	Comment
Host Bridge	2080h	n/a	2	Integrated in chipset
Graphic Controller	2081h	INTA# (IRQ9)	n/a	Integrated in chipset
Encryption Controller	2082h	INTA# (IRQ9)	n/a	Integrated in chipset
Ethernet Controller 2 (AD22)	1209h	INTB# (IRQ10)	1 ➔ X1-0	Intel 82551
Ethernet Controller 1 (AD23)	1209h	INTB# (IRQ10)	1 ➔ X1-1	Intel 82551
PCI/ISA bridge (AD24)	0628h	n/a	1 ➔ X1-2	IT8888
PCI/ISA bridge	2090h	n/a	n/a	Integrated in chipset
IDE Controller	209Ah	n/a	n/a	Integrated in chipset
Audio Controller	2093h	INTA# (IRQ9)	n/a	Integrated in chipset
USB Controller	2094h	INTD# (IRQ7)	n/a	Integrated in chipset
USB Controller	2095h	INTD# (IRQ7)	n/a	Integrated in chipset
PCI Slot 1	n/a	INTC# (IRQ7,9,10)	0 ➔ X2-0	PCI Expander 2
PCI Slot 2	n/a	INTC# (IRQ7,9,10)	0 ➔ X2-1	PCI Expander 2
PCI Slot 3	n/a	INTC# (IRQ7,9,10)	0 ➔ X2-2	PCI Expander 2

Tab. 3 PCI Devices

3.6. Hardware Interrupts

The AMD Geode LX800 chipset integrates two legacy 8259-compatible Programmable Interrupt Controllers (PIC). The registers of the PIC can be accessed through the I/O ports 020h and 021h resp. 0A0h and 0A1h.

Device	IRQ	PCI IRQ	Comment
8254 Timer	0	-	Legacy
Keyboard	1	-	Legacy
8259	2	-	Slave controller
UART	3	-	COM2
UART	4	-	COM1
UART	5	-	COM3
Free	6	-	Available on PC/104 bus (used for COM5 if available)
USB	7	PCI INTC# PCI INTD#	Do not used for with other devices
RTC	8	-	Legacy
Graphic Controller	9	PCI INTA# PCI INTC#	Shared with Encryption and Audio Controller
Ethernet	10	PCI INTB# PCI INTC#	Do not use with other devices
Free	11	-	Available on PC/104 bus (used for COM6 if available)
Mouse	12	-	Legacy
FPU	13	-	Legacy
IDE	14	-	Primary IDE channel
UART	15	-	COM4

Tab. 4 Hardware Interrupt Table

3.7. Peripheral Devices

3.7.1. Scope

The peripheral devices described in this chapter are the core features of the NETSBC-6A board. Meaning that they’re available on all the derivates. Special features implemented only on one special board are described in a separate chapter of this documentation.

3.7.2. Socket Memory

The NETSBC-6AC features a DIL32 socket (P9) for user insertable memory devices like SRAM, NVRAM and EEPROM products. Supported devices and corresponding configuration is listed in the table below, maximum access time allowed is 150 ns for all devices. Note that the Socket Memory base address, size and enabling must also be configured by software (BIOS).

Memory Type	Manufacturer and Order Code	J6 Setting (pins 8, 9,10,12 only)	J4 Setting
SRAM	**Static RAM (5V)**	**5V, Battery Backup enabled**	
128k x 8	Samsung: K6X1008C2D-DB70 Hitachi: HM628128BLP-7 STMicro: M68AF127BL70B6	8-10	2-3
512k x 8	Samsung: K6T4008C1C-DB70 Hitachi: HM628512BLP-7 Mitsubishi: M5M5408AP-70L	8-10	1-2
NVRAM	**Nonvolatile RAM (5V)**	**5V, Battery Backup disabled**	
32k x 8	ZMD: U637256DC70	9-10	2-3
32k x 8	Simtek: STK16C88-W45	9-10	2-3
NVRAM	**Nonvolatile RAM (3.3V)**	**3.3V, Battery Backup disabled**	
128k x 8	Simtek: STK16CA8-W45	10-12	2-3
EEPROM	**EEPROM (5V)**	**5V, Battery Backup disabled**	
32k x 8	Atmel: AT28C256(E)-15PC Catalyst: CAT28C256(H)P-15 Hitachi: HN58C256AP-10 ST: M28256-15BS Xicor: X28C256P-15	9-10	2-3
64k x 8	Catalyst: CAT28C512(H)P-15 SST: SST29EE512A-90-4C-PH Xicor: X28C512P-15	9-10	2-3
128k x 8	Atmel: AT28C010(E)-15PC SST: SST29EE010A-120-4C-PH Xicor: X28C010D-15	9-10	2-3

Tab. 5 Socket Memory Configuration

Important Note

Do not insert devices not listed. This could damage the hardware.

Important Note

For DiskOnChip device support plese contact the manufacturer.

Important Note

When inserting a 28 pin device into the 32 pin socket, pin 1 of the 28 pin device must be positioned at pin 3 of the DIL32 socket, otherwise the hardware may get damaged.

3.7.3. VGA Interface

The VGA signals are available on the High Density DVI-D connector connector P5 for direct connection of VGA compatible monitors. The controller uses the standard VGA register interface. All configuration is done by software (BIOS, VGA-BIOS).

3.7.4. DVI Interface

The DVI (Digital Visual Interface) signals are available on the High Density DVI-D connector P5 for direct connection of DVI compatible monitors. The signals from the SDVO (Serial Digital Video Out) port are converter into DVI signals from the The controller uses the standard VGA register interface. All configuration is done by software (BIOS, VGA-BIOS).

Device Connection

Pin Number	Signal	Remarks
1	DATA#2	
2	DATA2	
3	Shield 2/4	Connected to GND
4	DATA#4	Not connected
5	DATA4	Not connected
6	DDC_CLK	
7	DDC_DATA	
8	VSYNC	VGA Vertic. Sync
9	DATA#1	
10	DATA1	
11	Shield 1/3	Connected to GND
12	DATA#3	Not connected
13	DATA3	Not connected
14	VCC5	+5Vdc
15	GND	
16	HPDET	Hot Plug Detect
17	DATA#0	
18	DATA0	
19	Shield 0/5	Connected to GND
20	DATA#5	
21	DATA5	
22	Shield CLK	Connected to GND
23	CLK	
24	CLK#	
C1	VGA_RED	VGA Red
C2	VGA_GREEN	VGA Green
C3	VGA_BLUE	VGA Blue
C4	HSYNC	VGA Horiz. Sync
C5	VGA_GND	

Tab. 6 DVI-D connector P5

Important Note

Be careful when using the VGA or video signals on expansion boards. Special design and layout precautions must be met for these high speed analog signals.
Maximum cable length allowed for VGA connection is 15 m.
Use high quality VGA cables (with coaxial wires for RGB signals) for maximum EMI protection.

3.7.5. IDE/CompactFlash-Interface

The IDE interface is setup as Primary IDE Channel with standard PC address decoding and using hardware interrupt 14. It supports 2 external devices on a single connection, one configured as master the other as slave. Alternatively one external device may be replaced by an on board pluggable CompactFlash card. The IDE timing is setup by software (BIOS autodetection).
The IDE interface provides the following configuration options:

Configuration Options

Jumper	Configuration	Remarks
J6	Pin 2-4 open = on board CompactFlash is slave Pin 2-4 closed = on board CompactFlash is master	don't care if only external devices are connected.

Tab. 7 IDE Configuration Options

Device Connection

External IDE devices are connected through the standard 2x20 pin header P7. A CompactFlash card may be directly plugged in the on board CompactFlash connector P8.

Pin Number	Signal	Pin Number	Signal
1	RST#	2	GND
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	GND	20	NC
21	DRQ	22	GND
23	HIOW#	24	GND
25	HIOR#	26	GND
27	IOCHRDY	28	GND
29	DACK#	30	GND
31	IRQ	32	NC
33	HA1	34	PDIAG#
35	HA0	36	HA2
37	HCS0#	38	HCS1#
39	DASP#	40	GND
41	VCC	42	VCC
43	GND	44	NC

Tab. 8 IDE Connector P7 (2x22 pin)

Important Notes

Do not connect 2 external devices and a CompactFlash card together. This may damage the system and the IDE devices.

Note

The NETSBC-6A offers a 5V supply (not fused) for direct plugin IDE/CompactFlash adapters. Max. allowed current drawing is 100mA.

3.7.6. Serial Ports 1/2

Two serial ports are available. The serial ports have fixed base addresses of 3F8H for COM1 and 2F8H for COM2. COM1 uses hardware interrupt 4 and COM2 uses hardware interrupt 3.

Device Connection

The Serial Port COM1 is available on the DSUB9 connector P14A (bottom).
The Serial Port COM2 is available on the DSUB9 connector P15A (bottom).

Pin Number	Signal	Remarks
1	DCD*	
2	RXD	
3	TXD	
4	DTR*	
5	GND	
6	DSR*	
7	RTS*	
8	CTS*	
9	RI*	

Tab. 9 Serial Ports COM1 and COM2

Optional RS485 Interface on COM2 Port

Important Note
This chapter will be added in a future release.

3.7.7. Serial Ports 3/4

Two additonal serial ports are available on both IPC/NETSBC-6A2 and IPC/NETSBC-6AC. The serial ports have fixed base addresses of 3E8H for COM3 and 2E8H for COM4. COM3 uses hardware interrupt 5 and COM4 uses hardware interrupt 15.

Device Connection

The Serial Port COM3 is available on the DSUB9 connector P14B (top).
The Serial Port COM4 is available on the DSUB9 connector P15B (top).

Pin Number	Signal	Remarks
1	DCD*	
2	RXD	
3	TXD	
4	DTR*	
5	GND	
6	DSR*	
7	RTS*	
8	CTS*	
9	RI*	

Tab. 10 Serial Ports COM3 and COM4

Optional RS485 Interface on COM4 Port

Important Note
This chapter will be added in a future release.

3.7.8. Parallel Port

The Parallel Port is only available on an internal header.

Pin Number	Signal	Remarks
1	STROBE*	
2	PD0	
3	PD1	
4	PD2	
5	PD3	
6	PD4	
7	PD5	
8	PD6	
9	PD7	
10	ACK*	
11	BUSY	
12	PE	
13	SLCT	
14	AFD*	
15	ERROR*	
16	INIT*	
17	SLCTIN*	
18-26	GND	

Tab. 11 Parallel Port Connector J9

Important Note

The pin assignment on the Parallel Port connector J9 does not correspond with the standard LPT pin definition.

3.7.9. USB Interface

The NETSBC-6A features an OHCI/EHCI compatible USB Hostcontroller having assigned the base address and IRQ at boot time by the PCI-BIOS. Four channels are available where as channel 3 can be configured as a device.

Device Connection

The USB interface uses two dual USB connectors. USB2 and USB3 are also availabe on an internal header (J10).

P20 (top) Pin Number	USB channel 0 Signal	P20 (bottom) Pin Number	USB channel 1 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 12 USB Interface Connector P20

P21 (top) Pin Number	USB channel 2 Signal	P21 (bottom) Pin Number	USB channel 3 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 13 USB Interface Connector P21

The USB signals for channel 1 and 2 are also available on the internal header J10. A standard USB Flash Drive can be connected to this header.

J10 Pin Number	USB channel 2 Signal	P15 Pin Number	USB channel 1 Signal
1	VBUS	2	VBUS
3	D-	4	D-
5	D+	6	D+
7	GND	8	GND
9	Not connected	10	Not connected

Tab. 14 USB Interface Connector J10 (2x5pin)

3.7.10. PS/2 Keyboard/Mouse Interface

The keyboard signals are only available on an internal header J6. However a MiniDIN (PS/2 connector) can be mounted optionally instead of P21 (USB channels 2 and 3). The controller uses hardware interrupt 1 for the keyboard and hardware interrupt 12 for the mouse. The following configuration options are provided:

Configuration Options

Jumper	Configuration	Remarks
J6	Pin 1-3, 2-4 closed = Keyboard signals on P13 Pin 3-5, 4-6 closed = Mouse signals on P13	Only if P13 is mounted

Tab. 15 Keyboard/Mouse Configuration Options

Device Connection

The standard PS/2 connector P13 is not mounted by default. The PS/2 singals are available on the internal header J6 (2x5 pin). P13 is used (if available) for direct connection of the keyboard or mouse (depending on jumper configuration).

Pin Number	Signal	Pin Number	Signal
1	KBDATA	2	KBCLK
3	P3-1	4	P3-5
5	MDATA	6	MCLK
7	BM1 / P3-2	8	BM0 / P3-6
9	GND	10	+5V (not fused)

Tab. 16 Keyboard/Mouse internal Header J6 (2x5 pin)

Important Note

Do not connect the Boot Mode Pins on P3 or P4. These signals may only be used by the Boot Loader Key to start the Boot Loader.
The Boot Loader Key (BOOTPLUG) shortens Pin 3 and 6 of P13.

Important Note

Maximum cable length allowed for keyboard and mouse connection is 3 m.
Use shielded cables for maximum EMI protection.

3.7.11. Ethernet Interfaces

The NETSBC-6A features two PCI Ethernet 10/100 baseT controller having assigned the base address and IRQ at boot time by the BIOS. There are two LED's (yellow and green) integrated into the RJ45 connector. The green LED indicates speed. The LED will be on at 100Mbps and off at 10Mbps. The yellow" activity" LED indicates either transmit or receive activity. When activity is present, the LED is on; when no activity is present, the LED is off.
No configuration options are available for the ethernet device.

Device Connection

The Ethernet interface uses the standard RJ45 connector P18 and P19 for 100Ω shielded or unshielded Twisted Pair cabling.

Pin Number	Signal	Remarks
1	TX+	
2	TX-	
3	RX+	
4-5	line termination	
6	RX-	
7-8	line termination	

Tab. 17 Ethernet Twisted Pair Interface Connector P18 and P19 (RJ45)

3.7.12. Watchdog

The watchdog timer is configurable for 100 ms or 1.6 s timeout. Once timed out, it may activate the NETSBC-6A's hardware.

Configuration Options

Jumper	Configuration	Remarks
J6	Pin 4-6 open = 1.6 s Pin 4-6 closed = 100 ms	

Tab. 18 Watchdog Configuration Options

3.7.13. Power Supply

The processor and its peripherals are powered by a non-isolated, integrated power supply which generates all the necessary voltages.
See paragraph 6.2 for connection details.

Configuration Options

Switch	Configuration	Remarks
S12:1/2	on/off = external power on/off input pin off/on = external power fail input pin	P1:3

Tab. 19 Power Supervision Configuration Options

In some application it can be useful when the digital ground plane (GND) is connected to shield. In order to short circuit the two power planes two jumpers have to be placed on J16.

Jumper	Configuration	Remarks
J100	Pin 1-2 closed = shield and GND connected Pin 3-4 closed = shield and GND connected	

Tab. 20 Power plane short circuit

3.7.14. Power supervision

This feature is implemented on systems with #3 or higher.
The power management control unit (PCU) contains of RISC microcontroller and is implemented on the base board.
The PCU can be operated in two modes: power fail mode or remote on/off mode.
The following two chapters describe their functionality in detail.

3.7.15. Power Fail

In power fail mode the microcontroller monitors the external power fail signal. The state of power fail signal can be access through the status register, I/O 8200h.

Application example

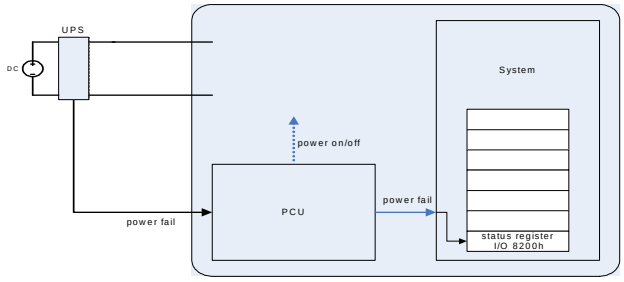

Fig. 7 Typical power fail application

The application has to poll the power fail flag and call different functions according to the state of the flag.

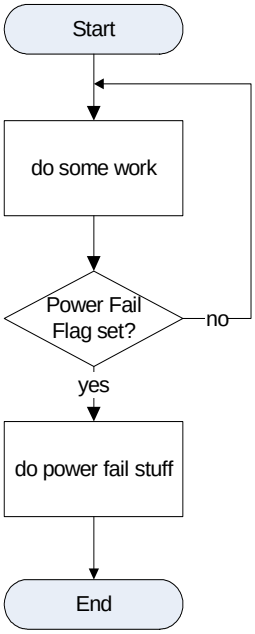

Fig. 8 Typical power fail flow

3.7.16. Remote On/Off

With the remote on/off function the system can be switched on and of through an external control signal. When active the internal software goes from the run state into the shutdown state. After a predefined timeout the PCU switches the main power supply off. The timeout can be configured through S14.

Config switch position	$t_{debounce\_on}$ On debouncing (setup)	$t_{debounce\_off}$ Off debouncing (hold)	$t_{startup}$ Hold time until switch off signal is routed to processor, if system is still booting	t_{hard_off} Timeout until switch off signal is generated from processor (after that hard off)
0	-	-	-	-
1	2 s	60 s	5 s	1 min
2	2 s	60 s	60 s	5 min
3	2 s	60 s	30 min	2 h
4	2 s	60 s	2 h	2 h
5 – F	N/a	n/a	n/a	n/a

Tab. 21 PCU timing configuration through S14

When switch S14 is in position 0 the PCU is in bypass mode.

Application example

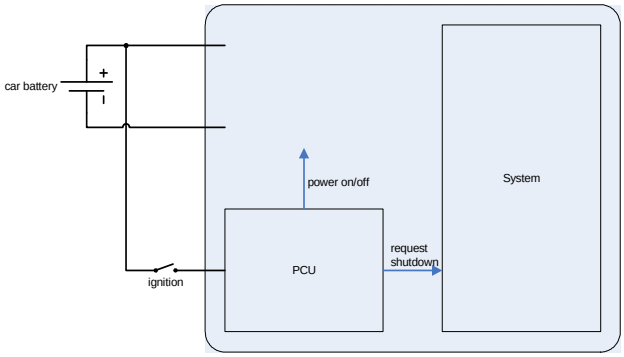

Fig. 9 Application example: CAR PC

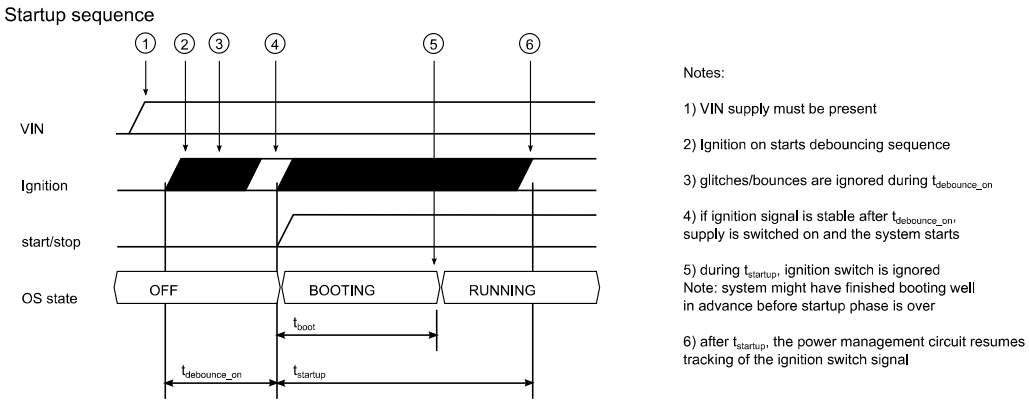

Fig. 10 Startup timing diagram

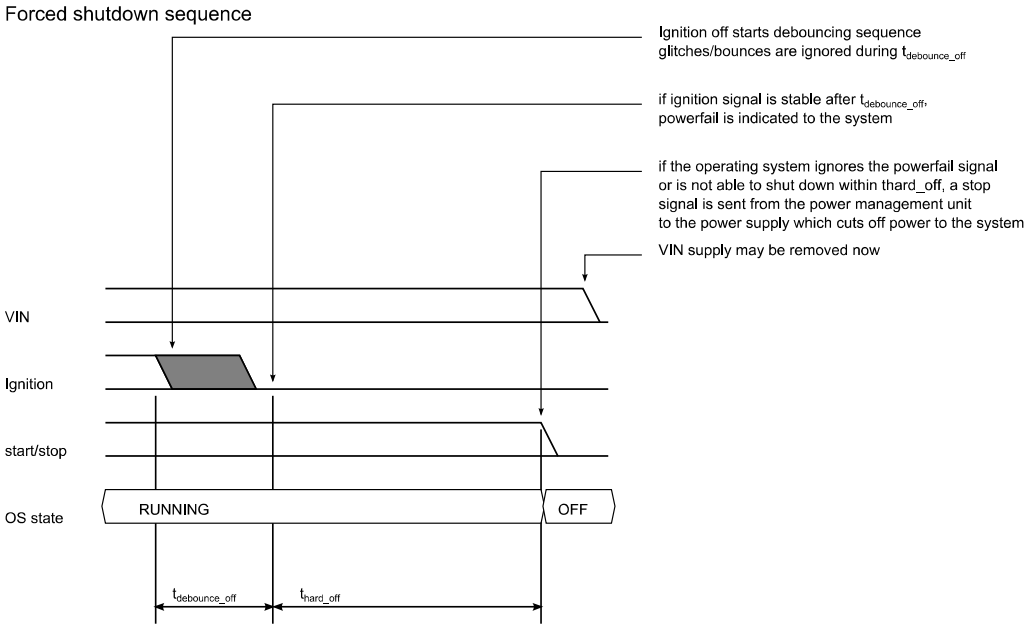

Fig. 11 Shutdown timing diagram

Important Notes

The operating system must support the remote on/off function.

Power Fail

A power fail can occur on two occasions: the external ipnut is pulled low or the power supply voltage drops below approx. 8.9Vdc.

Connector	Configuration	Remarks
P1:3	voltage > 2.5Vdc or left open = normal operation voltage < 2.5Vdc = power fail	S12:1/2 = off/on
P1:1-2	voltage >= 9.0Vdc = normal operation voltage < 8.9Vdc = power fail	S12:1/2 = off/on

Tab. 22 Power Fail

Remote On/Off

In some applications it is desirable that when a under-voltage event occurs that the systems shuts down.

Connector	Configuration	Remarks
P1:3	voltage > 2.5Vdc = normal operation voltage < 2.5Vdc or left open = shutdown	S12:1/2 = on/off
P1:1-2	voltage >= 9.0Vdc = normal operation voltage < 8.9Vdc = shutdown	S12:1/2 = on/off

Tab. 23 Remote On/Off

Important Note

The functions mentioned above are only available in systems with revision 3 or higher

3.7.17. Configurations Switches

There are two rotary Hex-Switches for customer use available, where only S1 can be accessed by removing the left side cover. The values can be read from a register at I/O address 820Ch

3.7.18. PC/104 Bus Interface

The PC/104 bus interface of the NETSBC allows expansion with a wide range of I/O and communications boards. The bus interface is described in the IEEE 996 and 996.1 standards documentation. The bus connector pinout is shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**. For single board applications only the power pins should be connected. See paragraph 7.1 for electrical specification.

Pin		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*
						A1	⊗	IOCHCK#	B1	⊗	GND
P11			P12			A2	⊗	SD7	B2	⊗	RESETDRV
1	⊗	GND	1	⊗	GND	A3	⊗	SD6	B3	⊗	+5V
2	⊗	no connection	2	⊗	+5V	A4	⊗	SD5	B4	⊗	IRQ9
3	⊗	no connection	3	⊗	TRIGGER*	A5	⊗	SD4	B5	⊗	-5V (not used)
4	⊗	Vbatt	4	⊗	STOP*	A6	⊗	SD3	B6	⊗	DRQ2
						A7	⊗	SD2	B7	⊗	-12V (not used)
						A8	⊗	SD1	B8	⊗	0WS#
D0	⊗	GND	C0	⊗	GND	A9	⊗	SD0	B9	⊗	+12V (not used)
D1	⊗	MEMCS16#	C1	⊗	SBHE#	A10	⊗	IOCHRDY	B10	⊗	(KEY)
D2	⊗	IOCS16#	C2	⊗	LA23	A11	⊗	AEN	B11	⊗	SMEMW#
D3	⊗	IRQ10	C3	⊗	LA22	A12	⊗	SA19	B12	⊗	SMEMR#
D4	⊗	IRQ11	C4	⊗	LA21	A13	⊗	SA18	B13	⊗	IOW#
D5	⊗	IRQ12	C5	⊗	LA20	A14	⊗	SA17	B14	⊗	IOR#
D6	⊗	IRQ15	C6	⊗	LA19	A15	⊗	SA16	B15	⊗	DACK3#
D7	⊗	IRQ14	C7	⊗	LA18	A16	⊗	SA15	B16	⊗	DRQ3
D8	⊗	DACK0#	C8	⊗	LA17	A17	⊗	SA14	B17	⊗	DACK1#
D9	⊗	DRQ0	C9	⊗	MEMR#	A18	⊗	SA13	B18	⊗	DRQ1
D10	⊗	DACK5#	C10	⊗	MEMW#	A19	⊗	SA12	B19	⊗	REFRESH#
D11	⊗	DRQ5	C11	⊗	SD8	A20	⊗	SA11	B20	⊗	SYSCLK
D12	⊗	DACK6#	C12	⊗	SD9	A21	⊗	SA10	B21	⊗	IRQ7
D13	⊗	DRQ6	C13	⊗	SD10	A22	⊗	SA9	B22	⊗	IRQ6
D14	⊗	DACK7#	C14	⊗	SD11	A23	⊗	SA8	B23	⊗	IRQ5
D15	⊗	DRQ7	C15	⊗	SD12	A24	⊗	SA7	B24	⊗	IRQ4
D16	⊗	+5V	C16	⊗	SD13	A25	⊗	SA6	B25	⊗	IRQ3
D17	⊗	MASTER#	C17	⊗	SD14	A26	⊗	SA5	B26	⊗	DACK2#
D18	⊗	GND	C18	⊗	SD15	A27	⊗	SA4	B27	⊗	TC
D19	⊗	GND	C19	⊗	(KEY)	A28	⊗	SA3	B28	⊗	BALE
						A29	⊗	SA2	B29	⊗	+5V
						A30	⊗	SA1	B30	⊗	OSC
						A31	⊗	SA0	B31	⊗	GND
						A32	⊗	GND	B32	⊗	GND

Tab. 24 PC/104 Bus Connectors PA/PB, PC/PD

Important Note

For proper operation ***all*** +5V and GND pins must be connected with short, low impedance lines to the main power supply.

Important Note

Do not connect bus drivers/receivers with integrated bushold circuit to the PC/104 signals. This may disturb proper operation of the NETSBC board or add-on boards.

The battery backup supply for the onboard Real Time Clock and SRAM must be connected to connector P11 as follows (also see **Fehler! Verweisquelle konnte nicht gefunden werden.**) :

Pin Number	Signal	Remarks
1	GND	
2	no connection	
3	no connection (KEY)	
4	Vbatt	

Tab. 25 External Battery Connector P11 (1x4 pin)

The user programmable output signals STOP* and TRIGGER* are available on connector P12. The signal levels are TTL compatible with maximum 4 mA sink and 2 mA source output current (also see **Fehler! Verweisquelle konnte nicht gefunden werden.**) :

Pin Number	Signal	Remarks
1	GND	
2	+5V	max. 10 mA
3	TRIGGER*	
4	STOP*	

Tab. 26 User Programmable Output Connector P12 (1x4 pin)

The TRIGGER* signal may be controlled by software or by a hardware timer, e.g. Timer Channel 2 Out (Speaker Drive) or Real Time Clock SQW output (see chapter 4).
A speaker may be connected to this signal if buffered with an external NPN transistor or inverting power driver.

3.7.19. PCI/104 Bus Interface

The PCI/104 bus interface of the NETIPC allows expansion with a wide range of I/O and communications boards. The bus interface is described in the IEEE 996 and 996.1 standards documentation. The bus connector pinout is shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**. See paragraph 7.1 for electrical specification.

Pin		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*
A			B			C			D		
1	⊗	GND	1	⊗	RESERVED	1	⊗	+5V	1	⊗	AD00
2	⊗	VI/O	2	⊗	AD02	2	⊗	AD01	2	⊗	+5V
3	⊗	AD05	3	⊗	GND	3	⊗	AD04	3	⊗	AD03
4	⊗	C/BE0#	4	⊗	AD07	4	⊗	GND	4	⊗	AD06
5	⊗	GND	5	⊗	AD09	5	⊗	AD08	5	⊗	GND
6	⊗	AD11	6	⊗	VI/O	6	⊗	AD10	6	⊗	M66EN
7	⊗	AD14	7	⊗	AD13	7	⊗	GND	7	⊗	AD12
8	⊗	+3.3V	8	⊗	C/BE1#	8	⊗	AD15	8	⊗	+3.3V
9	⊗	SERR#	9	⊗	GND	9	⊗	RESERVED	9	⊗	PAR
10	⊗	GND	10	⊗	PERR#	10	⊗	+3.3V	10	⊗	RESERVED
11	⊗	STOP#	11	⊗	+3.3V	11	⊗	LOCK#	11	⊗	GND
12	⊗	+3.3V	12	⊗	TRDY#	12	⊗	GND	12	⊗	DEVSEL#
13	⊗	FRAME#	13	⊗	GND	13	⊗	IRDY#	13	⊗	+3.3V
14	⊗	GND	14	⊗	AD16	14	⊗	+3.3V	14	⊗	C/BE2#
15	⊗	AD18	15	⊗	+3.3V	15	⊗	AD17	15	⊗	GND
16	⊗	AD21	16	⊗	AD20	16	⊗	GND	16	⊗	AD19
17	⊗	+3.3V	17	⊗	AD23	17	⊗	AD22	17	⊗	+3.3V
18	⊗	IDSEL0	18	⊗	GND	18	⊗	IDSEL1	18	⊗	IDSEL2
19	⊗	AD24	19	⊗	C/BE3#	19	⊗	VI/O	19	⊗	IDSEL3
20	⊗	GND	20	⊗	AD26	20	⊗	AD25	20	⊗	GND
21	⊗	AD29	21	⊗	+5V	21	⊗	AD28	21	⊗	AD27
22	⊗	+5V	22	⊗	AD30	22	⊗	GND	22	⊗	AD31
23	⊗	REQ0#	23	⊗	GND	23	⊗	REQ1#	23	⊗	VI/O
24	⊗	GND	24	⊗	REQ2	24	⊗	+5V	24	⊗	GNT0#
25	⊗	GNT1#	25	⊗	VI/0	25	⊗	GNT2#	25	⊗	GND
26	⊗	+5v	26	⊗	CLK0	26	⊗	GND	26	⊗	CLK1
27	⊗	CLK2	27	⊗	+5V	27	⊗	CLK3	27	⊗	GND
28	⊗	GND	28	⊗	INTD#	28	⊗	+5V	28	⊗	RST#
29	⊗	+12V	29	⊗	INTA#	29	⊗	INTB#	29	⊗	INTC#
30	⊗	+12V	30	⊗	REQ3#	30	⊗	GNT3#	30	⊗	GND

Tab. 27 PCI/104 Bus Connectors P6

Important Note

For proper operation ***all*** +5V and GND pins must be connected with short, low impedance lines to the main power supply.

Important Note

Do not connect bus drivers/receivers with integrated bushold circuit to the PCI/104 signals. This may disturb proper operation of the NETSBC board or add-on boards.

3.7.20. Factory Programming Header

The programmable logic devices on the NETSBC-6AC board are factory programmed using some pins of the internal header J5. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	TCK	do not use
3	TDO	do not use
5	TMS	do not use
7	TDI	do not use

Tab. 28 Factory Programming Header J5 (2x5 pin)

3.7.21. LPC Header

The internal LPC (Low Pin Count) bus is available on the header J3. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	AD0	do not use
2	AD1	do not use
3	AD2	do not use
4	AD3	do not use
5	FRAME#	do not use
6	RST#	do not use
7	CLK	do not use

Tab. 29 LPC J3 (1x7 pin)

3.7.22. Isolated Power Supply

Instead of the synchronous buck controller a DC/DC converter can be soldered onto the board for isolating the power supply. The input range will be reduced. For further information please contact the manufacturer

3.8. Peripherals Exclusively To IPC/COMPACT6-2A

3.8.1. General Information

The following peripherals are only available in the IPC/COMPACT6-2A system. These functions are implemented on the IPC/NETSBC-6A2 board.

3.8.2. Serial Ports 5/6

COM5 and COM6 are only available on the IPC/NETSBC-6A2. These two interface are only 4 pin and are only available on an internal header. The serial ports have fixed base addresses of 3A8H for COM5 and 2A8H for COM6. COM5 uses hardware interrupt 6 and COM6 uses hardware interrupt 11.

Device Connection

The Serial Port COM5 is available J7.
The Serial Port COM6 is available J8.

Pin Number	Signal	Remarks
1	nc	
2	nc	
3	RXD	
4	RTS#	SCOUT5#
5	TXD	
6	CTS#	SCIN5#
7	nc	
8	nc	
9	GND	
10	VCC	

Tab. 30 Serial Port COM5 on J7

Pin Number	Signal	Remarks
1	nc	
2	nc	
3	RXD	
4	RTS#	SCOUT6#
5	TXD	
6	CTS#	SCIN6#
7	nc	
8	nc	
9	GND	
10	VCC	

Tab. 31 Serial Ports COM6 on J8

3.9. Peripherals Exclusively To IPC/COMPACT6-2AC

3.9.1. General Information

The following peripherals are only available in the IPC/COMPACT6-2AC system. These functions are implemented on the IPC/NETSBC-6AC board.

3.9.2. CAN Interface

Important Note

This chapter will be added in a future release.

There is no firmware for the CAN interface. All setup functions have to be programmed by the user or configured by a third-party device driver.

Important Note

For detailed information and configuration options of the SJA1000 Stand Alone CAN Controller please refer to the appropriate documentation.

Memory Base Address Configuration

The memory base address is configured with S7. To set up the switch S7 proceed as followed:

S7/ appropriate address line	8 SA19	7 SA18	6 SA17	5 SA16	4 SA15	3 SA14	2 SA13	SA12 -SA0	1 I/O_MEM#
Segment:Offset									
0xE800:0	off	off	off	on	off	on	on	X	off
0xE000:0	off	off	off	on	on	on	on	X	off
0xD800:0	off	off	on	off	off	on	on	X	off
0xD000:0	off	off	on	off	on	on	on	X	off
0xC800:0	off	off	on	on	off	on	on	X	off
0xC000:0	off	off	on	on	on	on	on	X	off

Tab. 32 Memory Base Address Configuration

Note: Switch off: log. 1
Switch on: log. 0

S7 configures the segment address of the base address. Please make sure that the address range which you configure with SW301 is available on the bus. This can be done by checking (and changing) the BIOS configuration (refer to the documentation of the NETIPC Firmware).

Important Note

In standard PC-AT systems the address range 0xC000:0 .. 0xC7FF:F is reserved for the VGA BIOS. If the graphic controller on the CPU board is used then this address range can't be used.

I/O Base Address Configuration

The I/O base addresses cannot be configured. If the CAN controllers are operated in I/O mode the base addresses are 0x7600 and 0x7700 regardless how the switch is configured – except for S7-1 which defines the addressing mode.

S7/ appropriate address line	8 SA19	7 SA18	6 SA17	5 SA16	4 SA15	3 SA14	2 SA13	1 I/O_MEM#
Base address CAN1								
0x7600	X	X	X	X	X	X	X	on
Base address CAN2								
0x7700	X	X	X	X	X	X	X	on

Tab. 33 I/O Base Address Configuration

Note: Switch off: log. 1
Switch on: log. 0

Important Note

Some standard PC-AT peripherals are in the same I/O address range as the submodule. Please check your individual configuration for conflicts.

Interrupt Configuration

The interrupt for both CAN channels is configured via the rotary hex switch S9

S9	IRQ Number	Remarks
0	0	no IRQ
1	1	legacy interrupt – not usable
2	2	legacy interrupt – not usable
3	3	legacy interrupt – not usable
4	4	legacy interrupt – not usable
5	5	usable or COM3
6	6	can be used for CAN interface
7	7	can be used for CAN interface
8	8	legacy interrupt – not usable
9	9	PCI interrupt – not usable
A	10	PCI interrupt – not usable
B	11	can be used for CAN interface
C	12	legacy interrupt – not usable
D	13	legacy interrupt – not usable
E	14	legacy interrupt – not usable
F	15	usable or COM4

Tab. 34 Interrupt Selection

Important Note

It is required that all IRQs have to be checked for conflicts.

CAN Communication Interface

The IPC/COMPACT6-ML has two DSUB9 connectors for each channel:

- CAN1 IN: P16B (top)
- CAN1 OUT: P16A (bottom)
- CAN2 IN: P17B (top)
- CAN2 OUT: P17A (bottom)

Pin	Signal Designation	Signal
1	-	not used
2	CAN_L	CAN_L
3	CAN_GND	signal ground
4	-	not used
5	-	not used
6	-	not used
7	CAN_H	CAN_
8	-	not used
9	-	not used

Tab. 35 Pin Assignment of CAN Interface at P16 / P17 (bottom/top)

A 120Ω termination resistor is implemented on the base board module.

S10:1	Termination CAN1
on	active
off	not active

Tab. 36 Terminatino Resistor

S11:1	Termination CAN2
on	active
off	not active

Tab. 37 Termination Resistor

Important Note
S10:2 and S11:2 have no function.

3.10. Optional Functions

There are several functions on the NETSBC-6A which aren't implemented on the standard Syslogic product:

- isolated power supply
- RS485 interface at COM2 and COM6
- up to two isolated CAN interfaces
- 24bit LVDS (6bit/8bit) including brightness control
- AC97 audio port

For further technical information and customization details please contact Syslogic sales.

3.11. Hardware Limitations

3.11.1. PCI Bus Limitations

- Only 3.3V PCI bus
- PCI bus speed is limited to 33MHz
- COM5/COM6 are 4 pin interfaces (IPC/COMPACT6-2A resp. IPC/NETSBC-6A2 only)

3.11.2. ISA Bus Limitations

- The interrupt lines are pulled up with 8k2 resistors to Vcc (EISA specification) instead of 2k2 (IEEE 996)
- NMI (IOCHCK#) is not supported on the PC/104
- Only a predefined amount of I/O addresses are available on the PC/104 bus, please refer to the appropriate chapter for details

4 Programming Information

4.1. Overview

The programming of the NETSBC-6AC board is done with standard memory and I/O read and write operations. Most configuration options are handled by the BIOS. For detailled information refer to the NETSBC-6AC firmware documentation and other related documents as listed in paragraph 1.4.

4.2. Interrupt, Memory and I/O Resources

4.2.1. Interrupt Resources

Please refer to chapter 3.6 for the table showing the usage of the NETSBC-6AC's interrupts.

4.2.2. Memory Resources

The general memory layout is shown in paragraph 3.2.1. The configuration of the memory layout is done by programming Geode internal configuration registers and board configuration registers (see paragraph 4.2.3). This is done completely by the BIOS on system startup and must not be changed during operation. For operating systems requiring memory configuration (e.g. Windows CE) the memory layout shown in paragraph 3.2.1 must be considered.

4.2.3. I/O Resources

This paragraph describes only the NETSBC-6AC system register and support functions not directly related to a specific peripheral device. The general I/O layout is shown in paragraph 3.2.2. Peripheral devices are discussed in paragraph 0. Note that the Socket Memory related registers are programmed by the BIOS on system startup and must not be changed during operation except for the Socket Memory Window Mapping Register in case of user controlled memory mapping (allowing access to 512kbyte Socket Memory as eight 64kbyte blocks in the Socket Memory window below 1M in Real Mode).

Address	Device / Register	Remarks
8200h	Status Register	
8201h	Control Register	Reset state = 05H
8202h	Function ID Register	
8203h	reserved	do not write
8204h	Option ID Register	
8205h	Setup Register	Reset state = 00H
8206h	Revision ID Register	
8207h	Socket Memory Configuration Register	Reset state = 00H
8208h	Socket Memory Window Mapping Register	Reset state = 00H
8209h	Socket Memory Window Base Address Register	Reset state = D0H
820Ah	Boot Mode Input Register	
820Bh	I2C Register	for Temp Sensor
820Ch	Switch Register	do not write
820Dh	reserved	do not access
820F..82CFh	reserved	do not access
82E0h	Status Register	IPC/NETSBC-6AC only
82E1h	reserved	do not access
82E2h	Function ID Register	IPC/NETSBC-6AC only
82E3h	reserved	do not access
82E4h	Option ID Register	IPC/NETSBC-6AC only
82E5h	reserved	do not access
82E6h	Revision ID Register	IPC/NETSBC-6AC only
82E7..82FFh	reserved	do not access

Tab. 38 NETSBC-6AC System Registers

Status Register

Reading I/O Register 8200h:

D7	D6	D5	D4	D3	D2	D1	D0
OVERTMP*	LOBAT*	1	WDG*	ERRFLAG*	ATTFLAG*	ERRINT*	PF*

Description:

- PF*: Power Fail Status Flag
  0 = Power fail occured
  1 = No power fail occured
- ERRINT*: Error Interrupt Status
  0 = Error Interrupt pending on this module
  1 = no Error Interrupt pending on this module
- ATTFLAG*: Attention Status Flag (for polled applications)
  not used, returns 1
- ERRFLAG*: Error Status Flag (for polled applications)
  not used, returns 1
- WDG*: Watchdog Status Flag
  0 = Watchdog has timed out
  1 = Watchdog running or disabled
  Reset by issuing a hardware reset (see register 8204H)
- LOBAT*: Battery Status Flag
  0 = Battery voltage low
  1 = Battery voltage ok
- OVERTMP*: Temperatur Sensor Status Flag
  0 = programmed temperatur limit reached
  1 = temperatur ok (below limit)

Writing I/O Register 8200h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Control Register

Reading I/O Register 8201h:

D7	D6	D5	D4	D3	D2	D1	D0
TRIGGER	WDTRIG	WDNMI	STOP	*TRIGSRC*	FREEZE	ERREN*	ATTEN*

Description:

- ATTEN*: Attention Interrupt Enable
  not used, returns 1
- ERREN*: Error Interrupt Enable (IOCHCK* routed to NMI)
  0 = Error interrupt on NMI enabled (always enabled)
- FREEZE: not used, returns 1
- *TRIGSRC: NETIPC TRIGGER* Signal Source Select*
  always 1
- STOP: NETIPC STOP* Signal State
  0 = STOP* inactive (high)
  1 = STOP* active (low)
- WDNMI: Watchdog action Select
  0 = Watchdog timeout activates hardware reset
  1 = not supported
- WDTRIG: Watchdog Trigger
  any state change triggers the watchdog (timeout reset)
- *TRIGGER: Direct Control for NETIPC TRIGGER* Signal*
  always 1

Writing I/O Register 8201h:

D7	D6	D5	D4	D3	D2	D1	D0
TRIGGER	WDTRIG	WDNMI	STOP	*TRIGSRC*	FREEZE	ERREN*	ATTEN*

Description:

- ATTEN*: Attention Interrupt Enable
  not used
- ERREN*: Error Interrupt Enable (IOCHCK* routing to NMI)
  0 = enable Error interrupt on NMI (always enabled)
- FREEZE: not used
- *TRIGSRC: NETIPC TRIGGER* Signal Source Select*
  always write 1
- STOP: NETIPC STOP* Signal State
  0 = STOP* inactive (high)
  1 = STOP* active (low)
- WDNMI: Watchdog action Select
  always write 0
- WDTRIG: Watchdog Trigger
  any state change triggers the watchdog (timeout reset)

- TRIGGER: Direct Control for NETIPC TRIGGER* Signal
  (if enabled by TRIGSRC bit in Control Register)
  always write 1

The Trigger feature is not supported on the IPC/NETIPC-6 boards.

TRIGSRC	TRIGGER	TRIGGER* Source
0	0	Square Wave Output (SQW) of Real Time Clock Device
0	1	Timer (8254) Channel 2 Output gated with Port B bit 1 (Speaker Enable)
1	X	TRIGGER bit directly controls the TRIGGER* output

Tab. 39 TRIGGER* Source Selection

Function ID Register

Reading I/O Register 8202h:

D7	D6	D5	D4	D3	D2	D1	D0
FID7	FID6	FID5	FID4	FID3	FID2	FID1	FID0

Description:

- FID7..0: Function ID
  0101'0001 (51h) = general NETIPC board,
  subtype defined by Option ID Register

Writing I/O Register 8202h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Option ID Register

Reading I/O Register 8204h:

D7	D6	D5	D4	D3	D2	D1	D0
OPT7	OPT6	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0

Description:

- OPT7..0: Option ID
  1011'1000 (B8h) = IPC/NETSBC-6, 512MB (if FID = 51h)

Writing I/O Register 8204h:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X

Description:

- xxxxxxxx: Writing data A5h invokes a complete hardware reset (also clearing the Watchdog timeout status bit)

Setup Register

Reading I/O Register 8205h:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	0	0	0	0	0	0

Description:

- WDEN: Watchdog Enable
  0 = Watchdog disabled
  1 = Watchdog enabled (running)
- READY: NETIPC READY Signal State
  0 = READY inactive
  1 = READY active

Writing I/O Register 8205h:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0
- WDEN: Watchdog Enable
  0 = Watchdog disabled (cannot be disabled while running)
  1 = enable Watchdog
- READY: NETIPC READY Signal State
  0 = deactivate READY
  1 = activate READY

Revision ID Register

Reading I/O Register 8206h:

D7	D6	D5	D4	D3	D2	D1	D0
RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0

Description:

- RID7..0: Revision ID
  xxH = Logic Design revision ID (see Tab. 56)

Writing I/O Register 8206h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Socket Memory Configuration Register

Reading I/O Register 8207h:

D7	D6	D5	D4	D3	D2	D1	D0
SOCKEN	0	0	0	0	0	0	MSIZE

Description:

- MSIZE: Socket Memory Window Size (below 1 M)
  0 = 32 kbyte
  1 = 64 kbyte
- SOCKEN: Socket Memory Window Enable
  0 = Window disabled below 1 M
  1 = Window enabled below 1 M

Writing I/O Register 8207h:

D7	D6	D5	D4	D3	D2	D1	D0
SOCKEN	0	0	0	0	0	0	MSIZE

Description:

- MSIZE: Socket Memory Window Size (below 1 M)
  0 = 32 kbyte
  1 = 64 kbyte
- SOCKEN: Socket Memory Window Enable
  0 = disable Window below 1 M
  1 = enable Window below 1 M

Socket Memory Window Mapping Register

Reading I/O Register 8208h:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	MMR2	MMR1	MMR0

Description:

- MMR2..0: Socket Memory Window Mapping Bit 2..0
  enables mapping of eight 64 kbyte pages (= 512 kbyte)

Writing I/O Register 8208h:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	MMR2	MMR1	MMR0

Description:

- MMR2..0: Socket Memory Window Mapping Bit 2..0
  enables mapping of eight 64 kbyte pages (= 512 kbyte)

Socket Memory Window Base Address Register

Reading I/O Register 8209h:

D7	D6	D5	D4	D3	D2	D1	D0
1	1	MBAS5	MBAS4	MBAS3	MBAS2	MBAS1	MBAS0

Description:

- MBAS7..0: Socket Memory Window Base Address Bit 19..12
  range C0000..DBFFFh

Writing I/O Register 8209h:

D7	D6	D5	D4	D3	D2	D1	D0
1	1	MBAS5	MBAS4	MBAS3	MBAS2	MBAS1	MBAS0

Description:

- MBAS7..0: Socket Memory Window Base Address Bit 19..12
  range C0000..DBFFFh

Boot Mode Input Register

Reading I/O Register 820Ah:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	BM1	BM0

Description:

- BM1..0: Boot Mode Inputs
  0 = reserved (Factory Diagnostic Mode)
  1 = reserved
  2 = Boot Loader Mode
  3 = normal Operating Mode

Writing I/O Register 820Ah:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, do not write

I2C Register (for temperatur sensor control)

Reading I/O Register 820Bh:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	SCL	SDA	1	1	1	1

Description:

- SDA: Data Port Pin State
  0 = Pin State = Low
  1 = Pin State = High
- SCL: Clock Port Pin State
  0 = Pin State = Low
  1 = Pin State = High
- SDAO: Data Port Output Latch State
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output State
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)

Writing I/O Register 820Bh:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	X	X	X	X	X	X

Description:

- SDAO: Data Port Output Latch
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)

Switch Register

Reading I/O Register 820Ch:

D7	D6	D5	D4	D3	D2	D1	D0
S2_3	S2_2	S2_1	S2_0	S1_3	S1_2	S1_1	S1_0

Description:

- S2_3: Data 2^3
- S2_2: Data 2^2
- S2_1: Data 2^1
- S2_0: Data 2^0

- S1_3: Data 2^3
- S1_2: Data 2^2
- S1_1: Data 2^1
- S1_0: Data 2^0

Writing I/O Register 820Ch:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	Reserved

Description:

reserved: reserved, do not write

CAN Status Register

This register is only available on the IPC/COMPACT6-2AC and the IPC/NETSBC-6AC.

Reading I/O Register 82E0h:

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	CAN2_IRQ*	1	1	1	CAN-IRQ*

Description:

- CAN2_IRQ*: IRQ CAN channel 2
  0 = IRQ pending
  1 = no IRQ pending
- CAN1_IRQ*: IRQ CAN channel 1
  0 = IRQ pending
  1 = no IRQ pending

Writing I/O Register 82E0h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

reserved: reserved, always write 0

CAN FID Register

This register is only available on the IPC/COMPACT6-2AC and the IPC/NETSBC-6AC.

Reading I/O Register 82E2h:

D7	D6	D5	D4	D3	D2	D1	D0
FID7	FID6	FID5	FID4	FID3	FID2	FID1	FID0

Description:

- FID7..0: Function ID
  0110'1010 (6Ah) = IPC/NETSBC-6AC board,
  subtype defined by Option ID Register

Writing I/O Register 82E2h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

CAN Option ID Register

This register is only available on the IPC/COMPACT6-2AC and the IPC/NETSBC-6AC.

Reading I/O Register 82E4h:

D7	D6	D5	D4	D3	D2	D1	D0
IO_MEM2*	0	0	1	IO_MEM1*	0	0	1

Description:

- IO_MEM2*: Addressing mode CAN channel 2
  0 = I/O mode
  1 = Memory mode
- IO_MEM1*: Addressing mode CAN channel 1
  0 = I/O mode
  1 = Memory mode

Writing I/O Register 82E4h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

CAN Revision ID Register

This register is only available on the IPC/COMPACT6-2AC and the IPC/NETSBC-6AC.

Reading I/O Register 82E6h:

D7	D6	D5	D4	D3	D2	D1	D0
RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0

Description:

- RID7..0: Revision ID
  xxH = Logic Design revision ID (see Tab. 56)

Writing I/O Register 82E6h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

reserved: reserved, always write 0

4.3. Peripheral Devices

4.3.1. VGA-Interface

The VGA interface uses the standard PC/AT VGA register set. For detailled programming information please refer to the IBM PC/AT Technical Reference or similar documentation.
Low level programming is handled by the VESA compatible VGA-BIOS.

4.3.2. IDE-Interface

The IDE interface uses the standard PC/AT register set. For detailled programming information please refer to the IBM PC/AT Technical Reference, ATA/ATAPI standards (ANSI) or similar documentation.

4.3.3. Serial Ports

The Serial Port interfaces use the standard PC/AT register set. The Serial Port controller is compatible with the standard 16C550A UART with 16 byte receive and transmit FIFOs. For detailed programming information please refer to the IBM PC/AT Technical Reference, the Texas Instruments TL16C550C datasheet or similar documentation.

4.3.4. Keyboard/Mouse Interface

The Keyboard/Mouse interface uses the standard PC/AT register set. The keyboard controller is compatible with the standard Intel 82C42 device with integrated keyboard host controller firmware. For detailed programming information please refer to the IBM PC/AT and PS/2 Technical Reference, the Intel 82C42PC datasheet or similar documentation.

4.3.5. Ethernet Interfaces

On the NETSBC-6AC board the Ethernet interfaces use the Intel 82551 Ethernet Controller. For detailed programming information and drivers check www.syslogic.ch and www.intel.com
.

4.3.6. Temperature Sensor

The Temperator Sensor is built up using an LM75 compatible temperature sensor programmable through an I2C interface. The I2C interface programming is done through the I2C Register of the NETSBC-6AC. The LM75 can be accessed at the I2C address 00h. For detailled programming information please refer to the National Semiconductor LM75 datasheet or similar documentation.
Poweron default setting for OVERTMP* is 80°C chip temperature.

I2C Address	Device	Remarks
00h	LM75	

Tab. 40 I2C Address Space

4.3.7. Watchdog

The watchdog is disabled by default on poweron and must be enabled either by the BIOS or by the application program.
If watchdog programming is done from application software level, before enabling the watchdog by setting the WDEN bit in the NETSBC-6AC Setup Register.
The watchdog generates a hardware reset if it is not triggered within the configured timeout window by writing the WDTRIG bit in the NETSBC-6AC Control Register. The application must check the WDG* bit in the NETSBC-6AC Status Register uppon startup to identify the Watchdog as the source of the reset, and it must issue a hardware reset (by writing the value 0a5h to the NETSBC-6AC Option ID Register) to clear the WDG* flag. Otherwise the system resets again as soon as the Watchdog is started.
Sample code showing the initialisation and triggering of the watchdog is available in the free IPC/IOCOMSW-1A package.
For watchdog support on the BIOS level please consult the NETIPCFW firmware documentation. In this case initialisation is done by the BIOS on startup and triggering is done through BIOS API INT 15h calls.

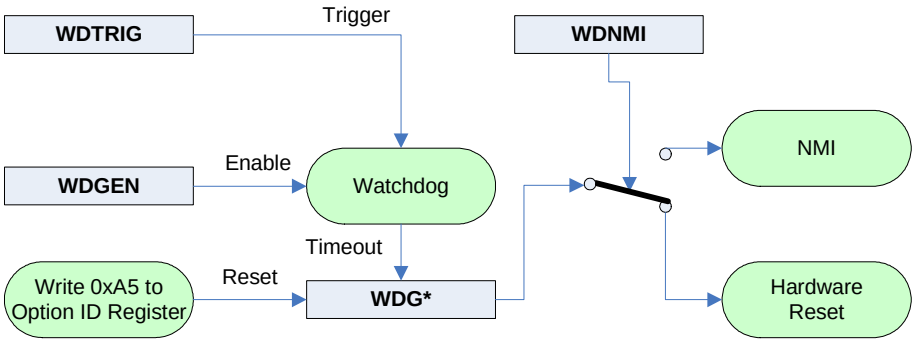

Fig. 12 Watchdog Blockdiagram

The watchdog can only initiate a hardware reset. The NMI option is not supported.

5 Enclosure, Assembly and Mounting

5.1. IPC/COMPACT6-ML Dimensions

The enclosure can house a complete industrial control system with many basic functions. The enclosure with its internal electronic system meets EMI/RFI electromagnetic standards according to the European ”CE”- requirements (see paragraph 1.5).

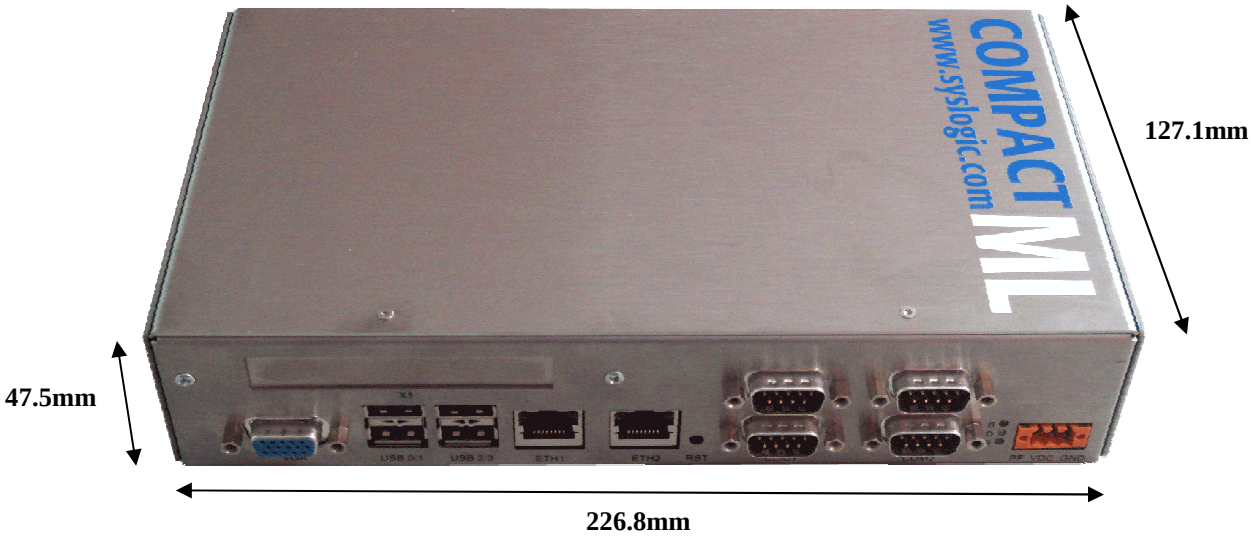

Fig. 13 IPC/COMPACT6-2AC

Important Notes

Before assembling the whole enclosure with the electronic modules please read through the following paragraphs containing information about the assembling of the system.

5.2. Internal Cabling

No internal cabling has to be done.

5.3. Serviceable Parts

The IPC/COMPACT6-ML contains two removable parts insie:

- Backup-Battery
- CompactFlash card (has to be ordered separately)

In order to exchange these parts, you must remove the cover by executing steps 1 and 2 of the following instructions.

Important Notes

When opening the enclosure you're about to handle ESD sensitive devices. Be sure that appropriate precautions have been made to your working environment. from its socket.

Important Notes

- The battery socket is coded, no wrong insertion of the backup battery is possible.
- Handle the flash memory module with care. In order to simplify the removal of the memoory module a small commercially available tape can be applied to the compact flash which allows an easy grab of the module.

1. Remove 4 torx screws (M2x5, BN3803) on the side of the case.

2. Remove the side cover.

3. Exchange the battery or the Compact Flash card.

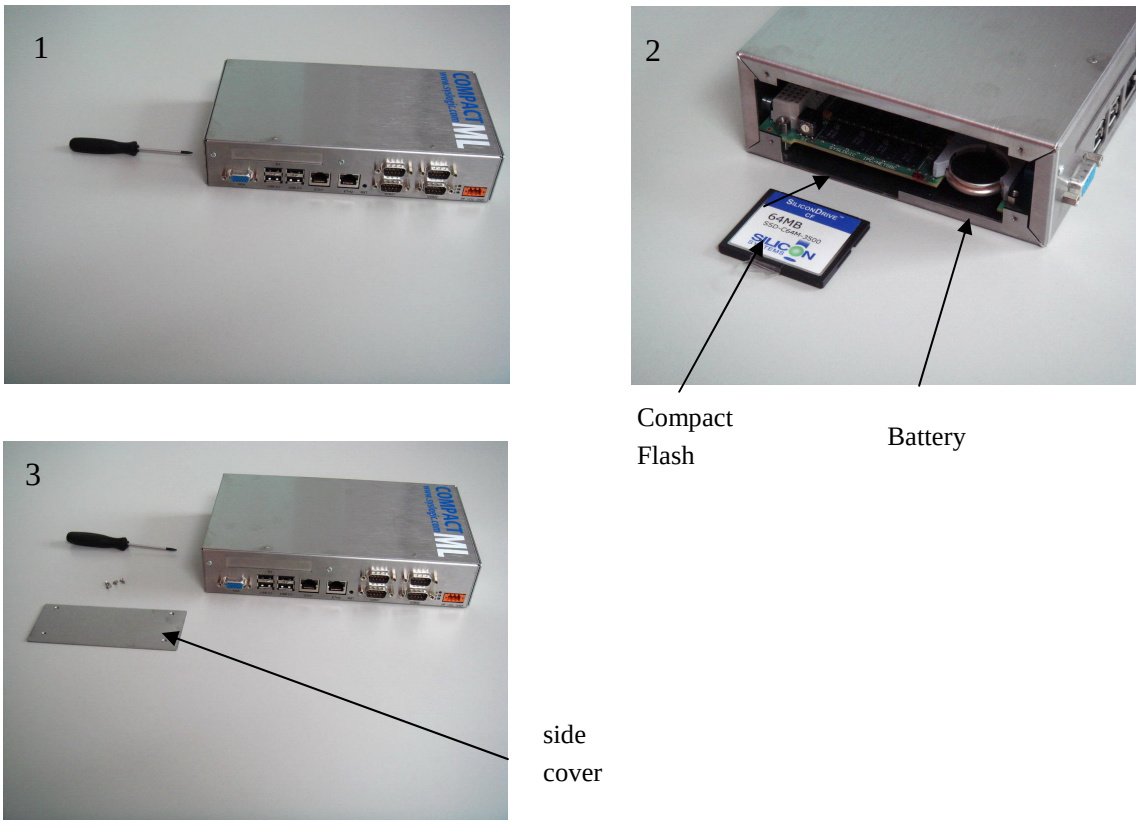

Fig. 14 Service of battery or Compact Flash card

5.4. Adding A PC/104 Compliant Board To Your System

5.4.1. General Information

The enclosure of the IPC/COMPACT6-ML has a break-out for a Weidmüller connector (S2L-SMT3.5/36/90LF3.2SNG, 179501). It can be used in together with a special cover (chapter 5.7).

Pos	Quantity	Part	Type/ Case	Manufacturer	Order Code
1	8	Torx screws	M2x4		
				Bossard	tbd
2	8	DSUB screws	UNC4-40/UNC4-40, SW4.5		
				Harting	09 67 001 9941
3	4	Torx screws	M2x4		
				Bossard	tbd
4	10	DSUB screws	UNC4-40/UNC4-40, SW4.5		
				Harting	09 67 001 9941
5	3	Torx screws	M3x15, plastic		
				Sibalco	Distin 3060PA-15
6	6	Plastic screws	M3x6, Plastic		
				Bossard	M3x6, BN1062, Polyamid 6.6
7	3	Torx screws	M3x6		
				Bossard	tbd

Tab. 41 Part List

Important Notes

Only one additional board can be mounted inside the IPC/COMPACT6-ML system.

Important Notes

When opening the enclosure you're about to handle ESD sensitive devices. Be sure that appropriate precautions have been made to your working environment. from its socket.

5.4.2. Removing the Electronic Boards

1. Remove both side cover of the enclosure described as in chapter 5.3 (pos. 1 and 2)

2. Remove the screws for the cover panel from the top and bottom (pos. 3).

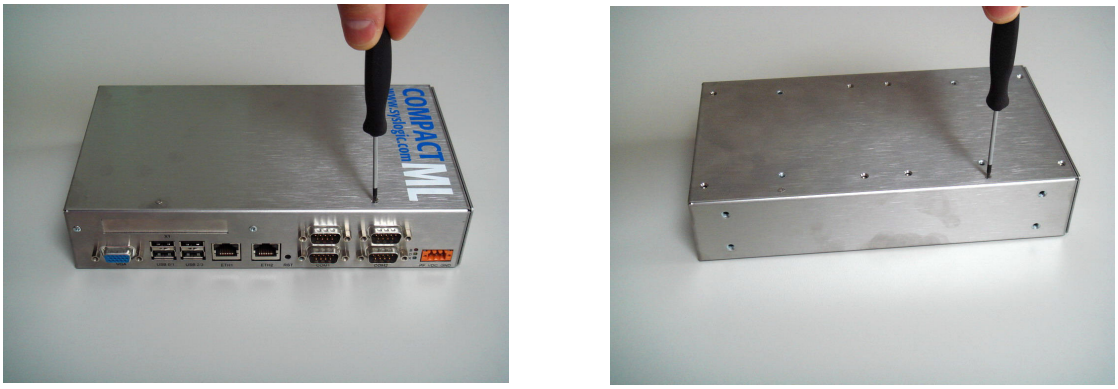

Fig. 15 Remove the cover screws

3. Carefully remove the cover.

Fig. 16 Remove the cover panel

4. Remove the DSUB screws from the front and the Torx screws from the bottom and from the front (pos. 4 and 5). Carefully remove the base board.

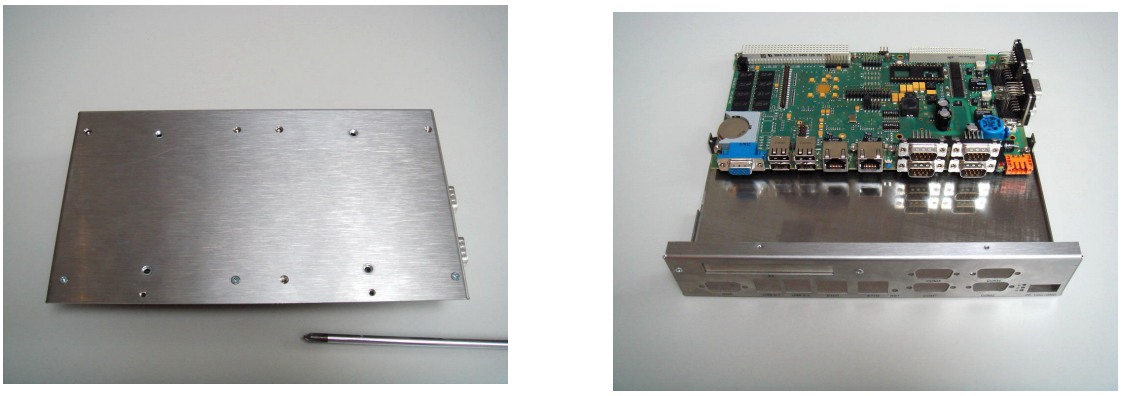

Fig. 17 Remove the base board

5.4.3. Mounting of the Add-on Board

1. In order to assemble the PC/104 compatible add-on board onto the base board three plastic PC/104 bolts (pos. 6) have to be screwed onto the PC/104 board with plastic screws (pos. 7).

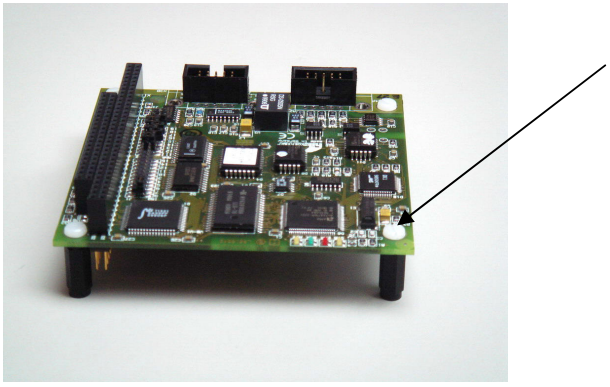

Fig. 18 PC/104 compliant board

2. Carefully plug the additional I/O board onto the board which has been previously removed from the enclosure. Be sure to check that all pins from the PC/104 bus are in position before you gently press down the board and distribute the pressure equally. Otherwise the electronic components could get damaged.

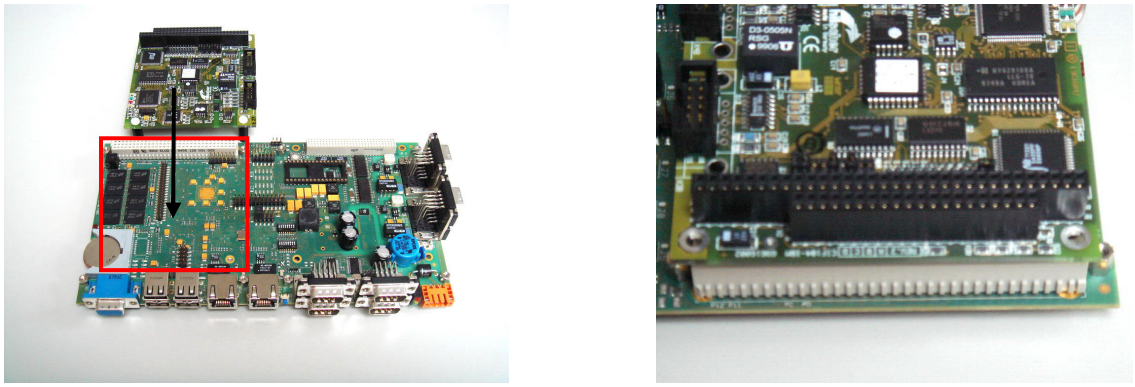

Fig. 19 Mounting the PC/104 compliant board onto the base board

3. Use the plastic screws (pos. 6) to fix the PC/104 board.

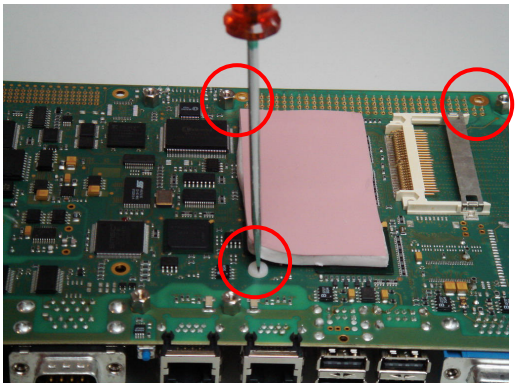

Fig. 20 Final mounting of the board

5.4.4. Final mounting

1. Carefully slide the electronic boards back into the enclosure. Be sure that all connectors fint into their break-outs in the front of the enclosure. Take great care while fitting in the electronic boards because the LEDs could get damaged.

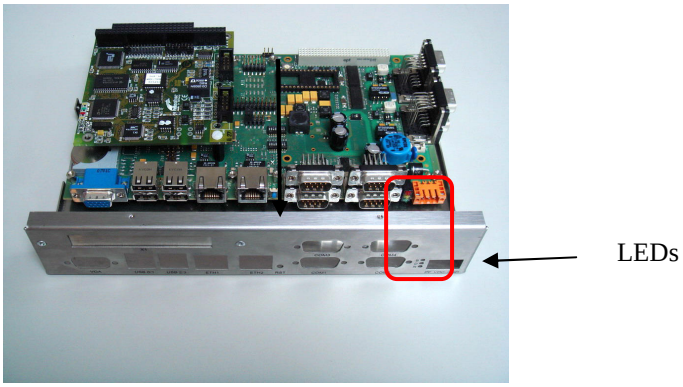

Fig. 21 Sliding the electronic boards back into the enclosure

2. Fix the electronics with the DSUB bolts and M2.5 screws (pos. 5 and 6) according to figure 12.

3. Mount the housing cover back on according to figure 10 (pos. 3):

4. The side covers can be mounted according to chapter 5.3.

5. If needed a special front panel can be mounted at the position of X1. Please check chapter 5.7 for details.

5.5. Adding A Standard PCI/104 Compliant Board To Your System

5.5.1. General Information

The enclosure of the IPC/COMPACT6-ML has a break-out for a Weidmüller connector (S2L-SMT3.5/36/90LF3.2SNG, 179501). It can be used in together with a special cover (chapter 5.7).

Pos	Quantity	Part	Type/ Case	Manufacturer	Order Code
1	8	Torx screws	M2x4		
				Bossard	tbd
2	8	DSUB screws	UNC4-40/UNC4-40, SW4.5		
				Harting	09 67 001 9941
3	4	Torx screws	M2x4		
				Bossard	tbd
4	10	DSUB screws	UNC4-40/UNC4-40, SW4.5		
				Harting	09 67 001 9941
5	3	Torx screws	M3x15, plastic		
				Sibalco	Distin 3060PA-15
6	6	Plastic screws	M3x6, Plastic		
				Bossard	M3x6, BN1062, Polyamid 6.6
7	3	Torx screws	M3x6		
				Bossard	tbd

Tab. 42 Part List

Important Notes

Only one additional board can be mounted inside the IPC/COMPACT6-ML system.

Important Notes

When opening the enclosure you're about to handle ESD sensitive devices. Be sure that appropriate precautions have been made to your working environment. from its socket.

5.5.2. Removing the Electronic Boards

1. Remove both side cover of the enclosure described as in chapter 5.3 (pos. 1 and 2)

2. Remove the screws for the cover panel from the top and bottom (pos. 3).

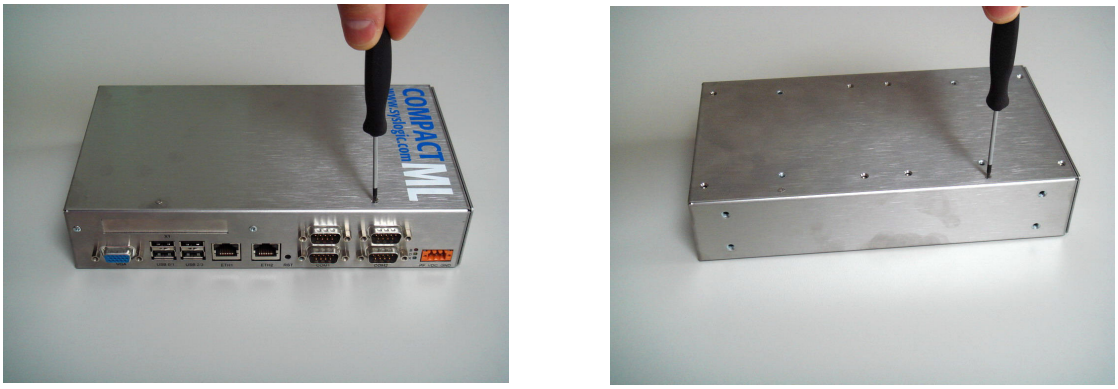

Fig. 22 Remove the cover panel

3. Carefully remove the cover.

Fig. 23 Remove the cover panel

4. Remove the DSUB screws fromt the front and the screws from the bottom and from the front (pos. 4 and 5). Carefully remove the base board.

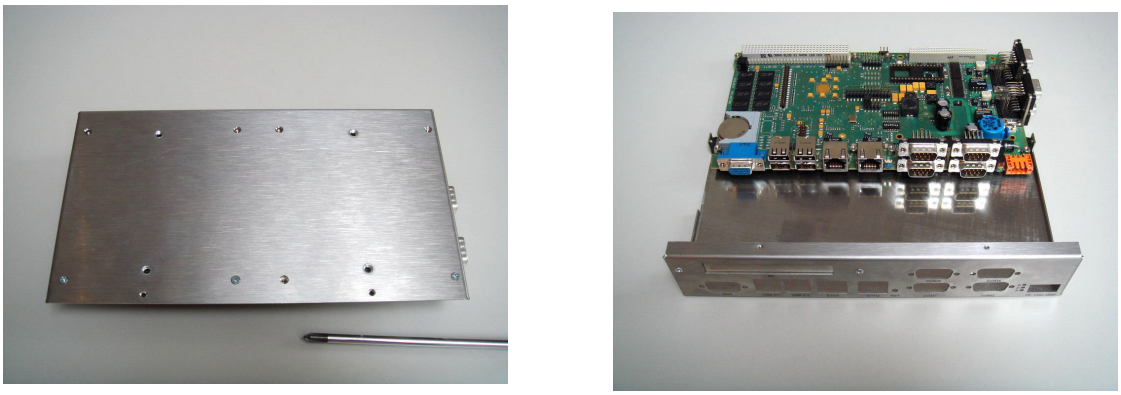

Fig. 24 Remove the base board

5.5.3. Mounting of the Add-on Board

1. In order to asemble the PCI/104 compatible add-on board onto the base board four plastic bolts (pos. 6) have to be screwed onto the PCI/104 board with plastic screws (pos. 7).

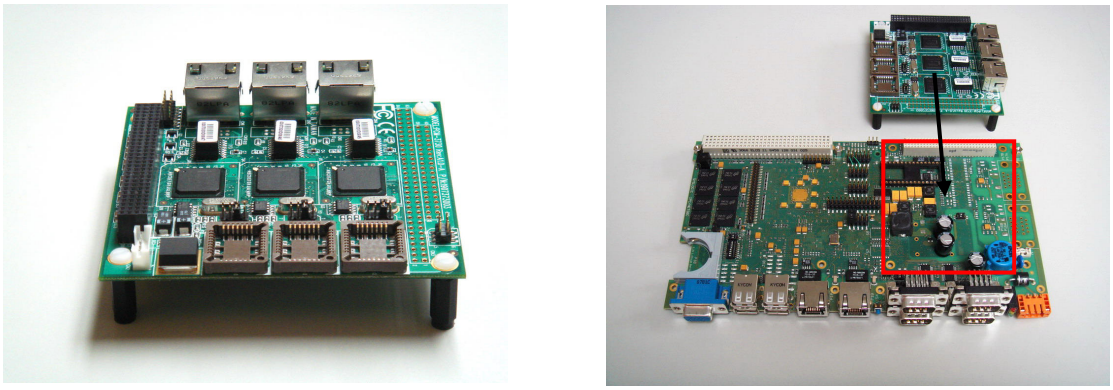

Fig. 25 PCI/104 compliant board

2. Carefully plug the additional I/O board onto the board which has been previously removed from the enclosure. Be sure to check that all pins from the PC/I/104 bus are in position before you gently press down the board and distribute the pressure equally. Otherwise the electronic compontents could get damaged.

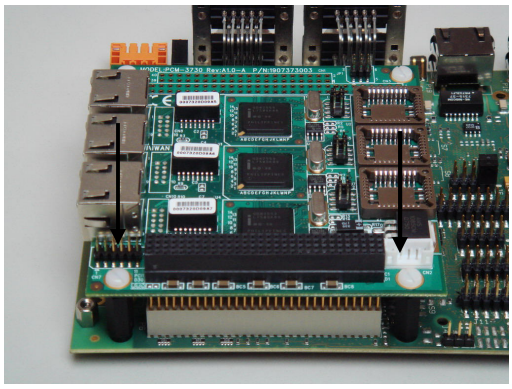

Fig. 26 Mounting the PCI/104 compliant board onto the base board

3. Use the plastic screws (pos. 6) to fix the PCI/104 board. The GapPad could be in the way of fixing the board with the plastic screws. Remove the silicon pad while screwing but don't forget to re-attach the GapPad.

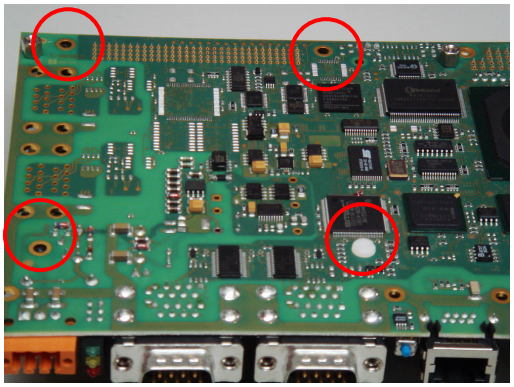

Fig. 27 Final mounting of the board

5.5.4. Final mounting

1. Carefully slide the electronic boards back into the enclosure. Be sure that all connectors fint into their break-outs in the front of the enclosure. Take great care while fitting in the electronic boards because the LEDs could get damaged.

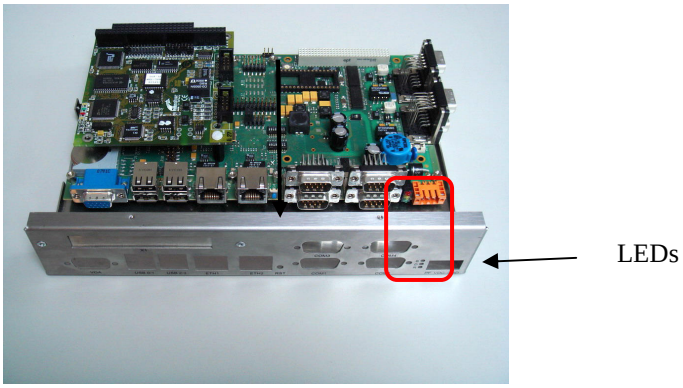

Fig. 28 Mounting the electronic boards into the enclosure

2. Fix the electronics with the DSUB bolts and M2.5 screws (pos. 5 and 6) according to figure 12.

3. Mount the housing cover back on according to figure 10 (pos. 3):

4. The side covers can be mounted according to chapter 5.3.

5. If needed a special front panel can be mounted at the position of X1. Please check chapter 5.7 for details.

5.6. Adding A PC/104 Compatible Add-on Board To Your System

5.6.1. General Information

The enclosure of the IPC/COMPACT6-ML has a break-out for a Weidmüller connector (S2L-SMT3.5/36/90LF3.2SNG, 179501). When mounting the additional board the standard PC/104 bolt positions are not being used.

Pos	Quantity	Part	Type/ Case	Manufacturer	Order Code
1	8	Torx screws	M2x4		
				Bossard	tbd
2	8	DSUB screws	UNC4-40/UNC4-40, SW4.5		
				Harting	09 67 001 9941
3	4	Torx screws	M2x4		
				Bossard	tbd
4	10	DSUB screws	UNC4-40/UNC4-40, SW4.5		
				Harting	09 67 001 9941
5	3	Torx screws	M3x15, plastic		
				Sibalco	Distin 3060PA-15
6	6	Plastic screws	M3x6, Plastic		
				Bossard	M3x6, BN1062, Polyamid 6.6
7	3	Torx screws	M3x6		
				Bossard	tbd
8	2	Lens screws	M2.5x6		
				Bossard	M2.5x6, BN3334, vzi-blau, Form Z
9	2	Reinforced rib washer	M2.5		
				Bossard	BN14083
10	2	Bolts	M2.5x18.7		
				Sibalco	Distinex 2550M-18.7
11	2	PCB card holder			
				Fischer	VS 3, 241761.8
				Rittal	3685.198
				Schroff	60807-181
12	2	Raised c'sunk screws	M2.5x4, DIN965A		
				Bossard	M2.5x4, BN388, vzi-blau
13	2	Lens screws	M2.5x6, DIN7985A		
				Bossard	M2.5x6, BN3334
14	2	Reinforced rib washer	M2.5		
				Bossard	BN14083

Tab. 43 Part List

Important Notes

Only one additional board can be mounted inside the IPC/COMPACT6-ML system.

Important Notes

When opening the enclosure you're about to handle ESD sensitive devices. Be sure that appropriate precautions have been made to your working environment. from its socket.

5.6.2. Removing the Cover

1. Remove both side cover of the enclosure described as in chapter 5.3 (pos. 1 and 2)

2. Remove the screws for the cover panel from the top and bottom (pos. 3).

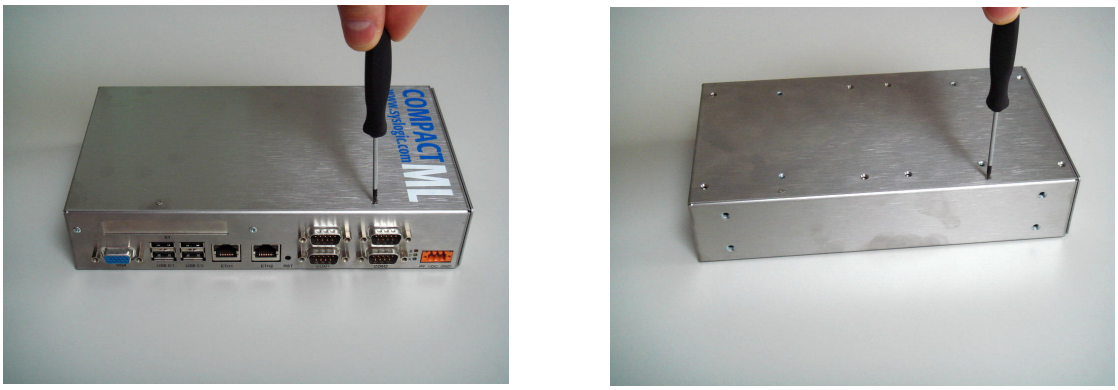

Fig. 29 Remove the cover panel

3. Carefully remove the cover.

Fig. 30 Remove the cover panel

5.6.3. Mounting the Add-on Board

1. Assemble the PCB card holder (pos. 11) with a screw (pos. 13) and washer (pos. 14) on both sides.

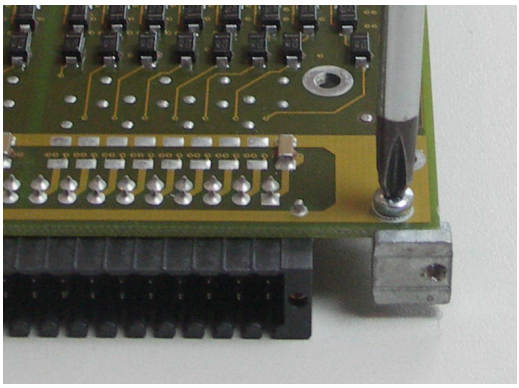

Fig. 31 Mounting the PCB card holder

2. If your add-on board has a Weidmüller connector at the front the cover at the front of the enclosure has to be removed.

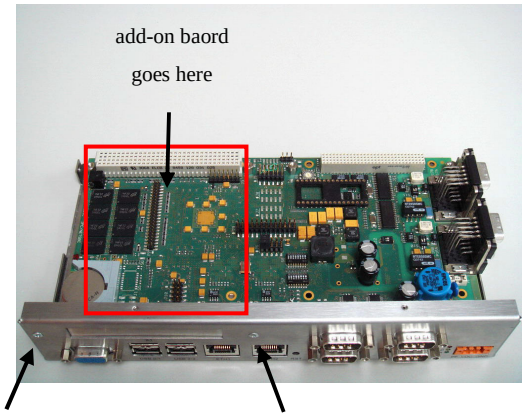

Fig. 32 Remove front cover

3. Remove the two hexagonal nuts fix the board with two bolts (pos. 10). To prevent the bolts (between PCB and enclosure) from spinning they should be fixed from the opposite side.

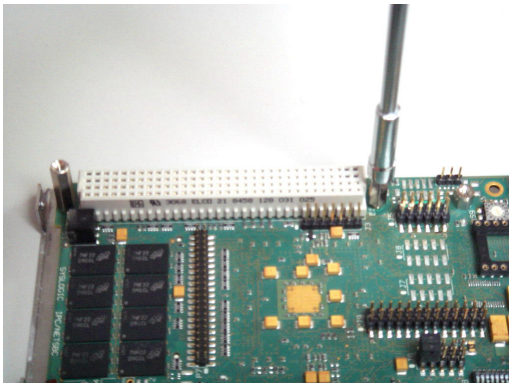

Fig. 33 Mounting the bolts

4. Carefully plug the additional I/O board onto the board which have been previously removed from the enclosure. Be sure to check that all pins from the PC/104 bus are in position before you genlty press down the board and distribute the pressure equally. Fix the add-on board with the screws (pos. 8) and the appropriate washer (pos. 9).

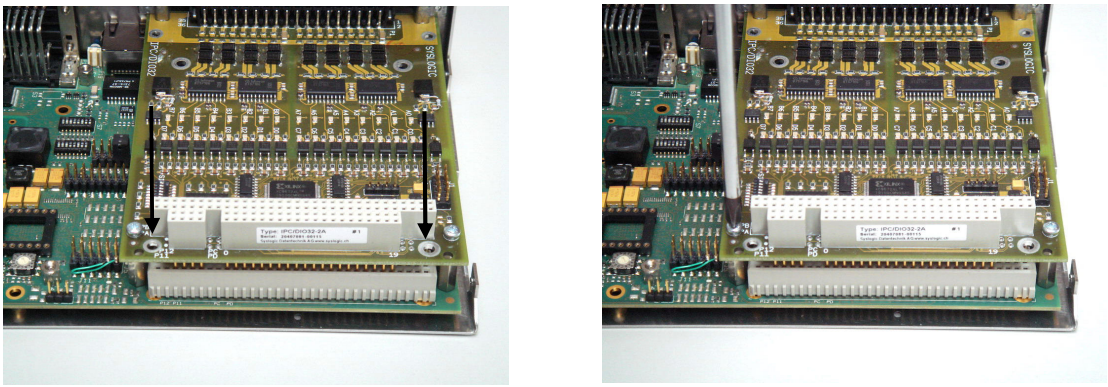

Fig. 34 Mounting the PC/104 compatible board

5. Fix the add-on board to the front with two screws (pos. 12).

Fig. 35 Fixing the add-on board

5.6.4. Final mounting

1. Carefully slide the electronic boards back into the enclosure. Be sure that all connectors fint into their break-outs in the front of the enclosure. Take great care while fitting in the electronic boards because the LEDs could get damaged.

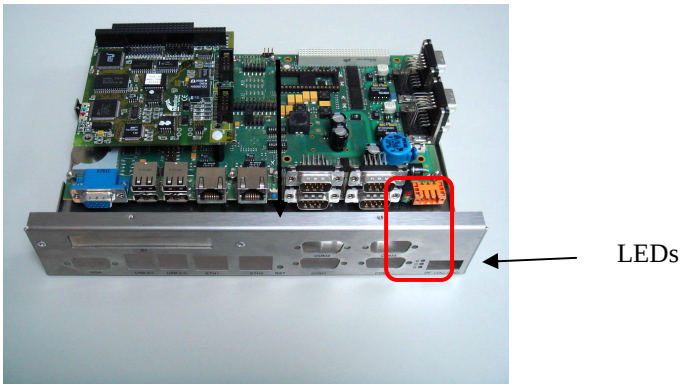

Fig. 36 Mounting the electronic boards into the enclosure

2. Fix the electronics with the DSUB bolts and M2.5 screws (pos. 1 and 2) according to figure 12.

3. Mount the housing cover back on according to figure 10 (pos. 3):

4. The side covers can be mounted according to chapter 5.3.

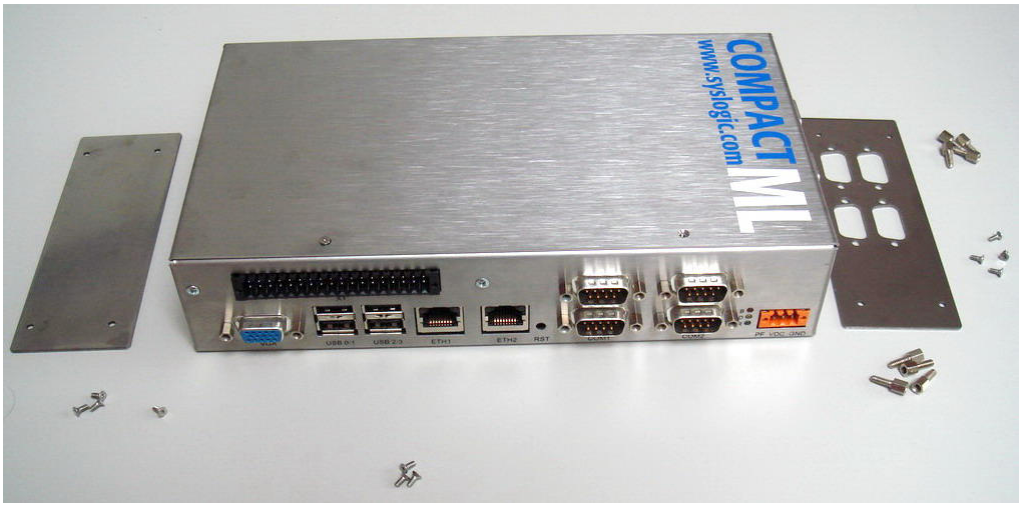

Fig. 37 Mounting the electronic boards into the enclosure

5. If needed a special front panel can be mounted at the position of X1. Please check chapter 5.7 for details.

5.7. Front Panel Options

There are two different cover panels with one or two DSUB9 break-outs can be mounted instead of the default panel.

Fig. 38 Cover panels

5.8. Final mounting of the enclosure

As mentioned in chapter 1.4.1 there for additional mounting kits which have to be ordered separately. The mounting kits help to install the IPC/COMPACT7-ML into your electric control cabinet. For detailed mechanical drawings please contact the manufacturer.

Important Notes

Be sure to use the correct screws; screws which are too long can damage the boards inside of the enclosure.

5.8.1. Rear mounting

Product order code: IPC/MKITCP-1B
Document order code: DOC/IPC_MKITCP-1BE

Fig. 39 Rear mounting of the IPC/COMPACT6-ML (product image may vary)

5.8.2. Vertical bottom mounting

Product order code: IPC/MKITCP-2A
Document order code: DOC/IPC_MKITCP-2AE

Fig. 40 Vertical bottom mounting of the IPC/COMPACT6-ML (product image may vary)

5.8.3. Horizontal bottom mounting

Product order code: IPC/MKITCP-2C
Document order code: DOC/IPC_MKITCP-2CE

Fig. 41 Horizontal bottom mounting of the IPC/COMPACT6-ML (product image may vary)

5.8.4. DIN rail mounting

Product order code: IPC/MKITCP-2E
Document order code: DOC/IPC_MKITCP-2EE

Fig. 42 One possible way of mounting the IPC/COMPACT6-ML onto the DIN-Rail (product image may vary)

6 Installation and Cabling

6.1. Introduction

Installation and cabling of the IPC/COMPACT6-ML system has to be done with great care; the correct cabling is essential for high operational reliability and the correct grounding is necessary for protection. To meet the requirements of "CE"-certification all cables have to be shielded. The enclosure has to be connected to ground via the DIN-rail.

Important Notes

To meet the requirements of RFI "CE"-cerification, correct mounting, installation and cabling of the IPC/COMPACT6-ML system according to these guidelines is absolutely necessary.

6.2. Powering the IPC/COMPACT6-ML System

The "logic voltage", i.e. the power driving the electronic circuits (CPU and base board) is applied from a 24VDC power supply (10VDC...30VDC). The internal power supply converts the input voltage to the logic voltage level. Remember that the power supply is unisolated. For an isolated version please contact the manufacturer. The input voltage is applied with a 3 or 4 pin Weidmüller connector, depending on the product version:

Pin Number	Signal	Remarks
1	+24VDC	+10V..+30V
2	+24VDC_AUX	Additional, permanent power supply
3	GND	Ground (/shield)
4	Power Fail/Remote on/off	Power Fail input

Tab. 44 Power supply connector P1 (2x2 pin, product version #4.x)

Pin Number	Signal	Remarks
1	GND	Ground
2	+24VDC	+10V..+30V
3	Power Fail	Power Fail input

Tab. 45 Power supply connector P1 (1x3 pin, product version #1-3)

The connector can be ordered directly at your Weidmüller distributor.

Order Code	Type
1001270000	B2L 3.5/04/180F (2x4 pin)
1606650000	BL3.5/3F (1x3 pin)

Tab. 46 Weidmüller power connector

For normal operation the external power supply has to be connected to +24VDC and GND of the connector P1.
See paragraph 3.7.14 and 3.7.15 for use of power fail or remote on/off signal.
When selecting the 24VDC power supply the maximum power dissipation of the system has to be considered.

Important Notes

Please make sure that the input voltage does not exceed 30V otherwise the base board could get damaged. If the input voltage drops below 10V the system doesn't work properly, correct operation cannot be guaranteed. The best efficiency of the power supply can be achieved if the external input voltage is around 24V. Therfore the power loss of the power supply circuitry is at its minimum. When operating the system at high temperatures please make sure that the power supply is around 24V.

The power fail and external shutdown functions (pin 3) are only available on systems with revision 3 or higher.

6.3. Cabling the Interfaces

Fig. 43 Front view with connector markings (image may vary)

Connector Marking	Interface Type
VGA	CRT
USB0/1	USB0 (bottom) / USB1 (top)
USB2/3	USB2 (bottom) / USB3 (top)
ETH1	Ethernet 1 (PCI device 13)
ETH2	Ethernet 2 (PCI device 12)
RST	Reset button
COM1	COM1: RS232
COM2	COM2: RS232 (or RS485)
COM3	COM3: RS232
COM4	COM4: RS232 (or RS485)
X1	Expansion Slot
red LED	(B): Busy
yellow LED	(D): Disk
green LED	(R): Run
VAUX PF VDC GND	Power Supply

Tab. 47 IPC/COMPACT6-2AC: Connectors

Fig. 44 Sidet view with connector markings (IPC/COMPACT6-2AC only)

Connector Marking	Interface Type
CAN1 (top)	CAN1 In
CAN1 (bottom)	CAN1 Out
CAN2 (top)	CAN2 In
CAN2 (bottom)	CAN2 Out

Tab. 48 IPC/COMPACT6-2AC: Connectors

6.4. Grounding

In some cases it is recommended to connect the shields of the cables to chassis potential at the entry point into the housing cabinet as shown in Fig. 45. If the cables enter a hermetically closed cabinet, use special 360 degree metal clamps (RFI protected types which contact to the cable shield).

Important Notes

Grounding of the cables shields using "pig-tail wires" are not recommended because of their high impedance at high frequencies. It is better to clamp the shields onto a grounded copper rail.

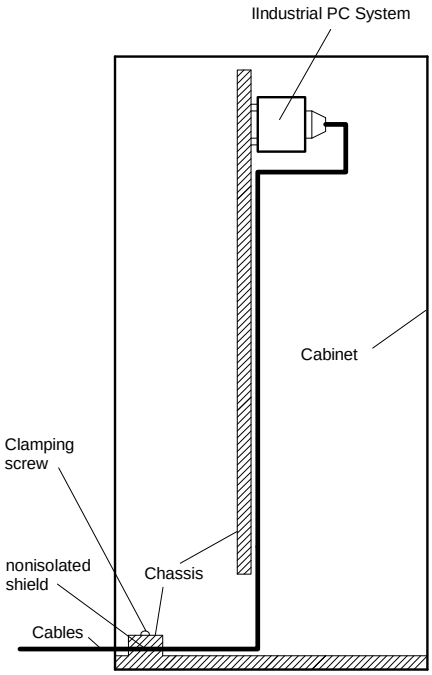

Fig. 45 Additional grounding of the cable shields at the entry point of a cabinet.

6.5. Cabling of Communication Links

If the communication ports are unisolated ports, cable shields have to be connected to chassis potential on both sides of the interconnection cable. If the cable is very long, a thick copper wire (10 mm^2) for potential adjustment is highly recommended. Fig. 46 shows an non isolated system with common chassis ground.

Some of the communication ports are galvanically isolated ports (for more information please refer to the documentation of the base board and the CPU board): in such cases the shield of the interconnection cable must be wired to chassis potential only on one side of the cable. Fig. 47 shows an isolated system with independent grounds.

Important Notes

Grounding of cable shields using "pig-tails wires" are not recommended because of their high impedance at high frequencies. It is recommended to clamp the shields onto a grounded copper-rail.

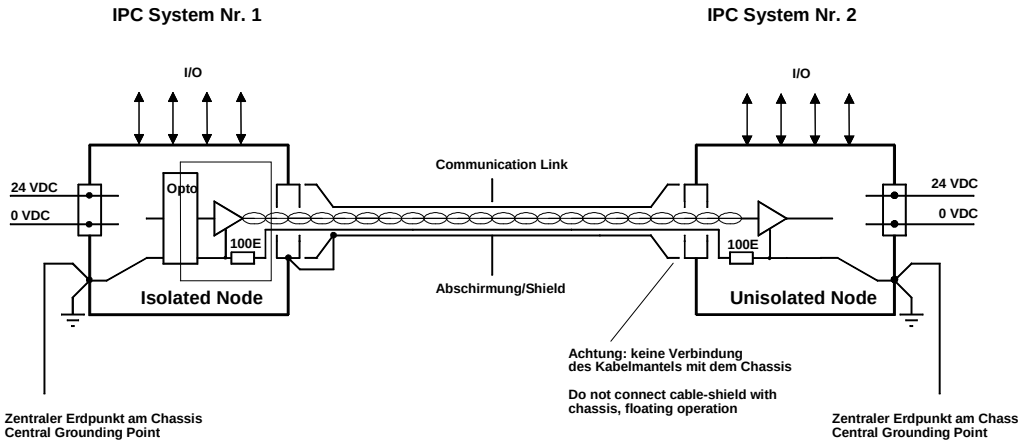

Fig. 46 Non isolated communication link with common chassis potential

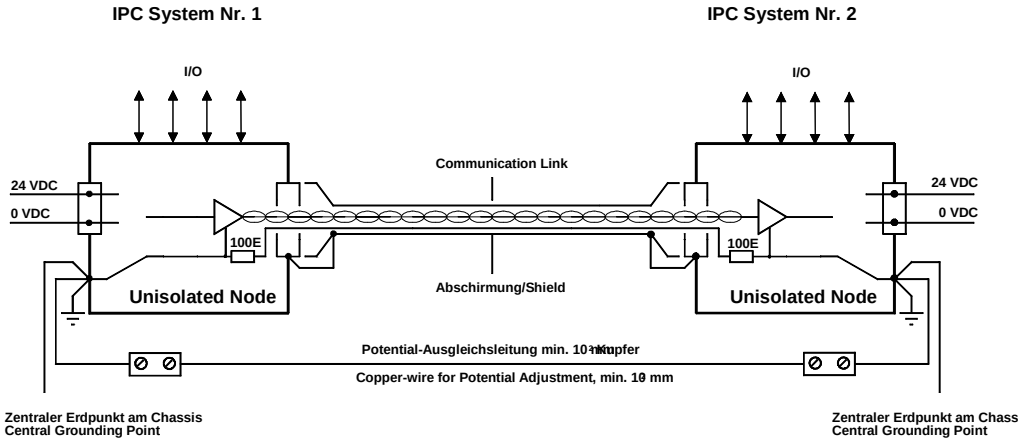

Fig. 47 Isolated communication link

7 Technical Data

7.1. Electrical Data

Important Note

Do not operate the IPC/COMPACT6-ML outside of the recommended operating conditions. Otherwise lifetime and performance will degrade. Operating the board outside of the absolute maximum ratings may damage the hardware.

Absolute Maximum Ratings (over free-air temperature range)

Parameter	Symbol	min	nom	max	Unit
internal power supply voltage	Vcc	-0.5		5.5	Vdc
isolation logic to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation RJ45 to logic (AC, 60s, 500m a.s.l., Ta=25°C)		1500			Vrms
isolation RJ45 to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		1000			Vdc
creepage distances:					
logic to chassis and PCB boarder		1.0			mm
logic to PC/104 mounting holes		0.5			mm
RJ45 to logic		2.5			mm
RJ45 to chassis and PCB boarder		2.0			mm
storage temperature range	Tst	-40		90	°C

Tab. 49 General Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Symbol	min	nom	max	
external supply voltage	Vext	10.0	24.0	30.0	Vdc
battery backup voltage (Io=100µA)	Vbatt	2.70	3.00	3.60	Vdc
PS/2 connector (P3/P4) power load (+5V)	Ips2			200	mA
operating free-air temperature range (no additional module)	Ta	0		55	°C
operating free-air temperature range (with additional module, 3.8W)	Ta	0		50	°C
maximum power load of additional module [1]				3.8	W

Tab. 50 General Recommended Operating Conditions

[1] Only one module can be mounted inside the IPC/COMPACT6-ML.

Electrical Characteristics (over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	Typ	max	Unit
external supply current @ 10Vdc	Iext		1.03	1.08	A
full load power dissipation @ 10Vdc	Pmax		10.69	10.78	W
external supply current @ 24Vdc	Iext		0.45	0.45	A
full load power dissipation @ 24Vdc	Pmax		10.83	10.86	W
Power Fail					
- inactive state	PFhigh	2.7	Vext	Vext	V
- active state	Pflow	-0.5	0	2.3	V
- sinking current [1]	Isink	1		3	mA
Remote on/off					
- on	ENon	8.5	Vext	Vext	V
- off	ENoff	-0.5	0	7.1	V
- driving current [2]	Idrive	1		3	mA
Vbatt loading (Vcc=0V, without SocketMemory)	Ibat(off)		3.5	10.0	uA
Vbatt loading (Vcc=5V)	Ibat(on)		1.5	4.0	uA
LOWBAT* trip point		2.35	2.5	2.65	V
VRT trip point (RTC Valid RAM and Time Flag)			2		V

Tab. 51 General Electrical Characteristics

[1] External device has a open collector/drain output.
[2] External device has to drive each logic level.

Switching Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	nom	max	
processor clock	pclk			500	MHz
memory clock (DDR400)	mclk			200	MHz
COM1/2 baud rate				115.2	kbaud
COM3/4 baud rate				115.2	kbaud
Watchdog timeout (short period)	Tw	70	100	140	ms
Watchdog timeout (long period)	Tw	1.0	1.6	2.25	s
Timer base clock 1	fclk1		14.318		MHz
Timer base clock 1 accuracy				+/-100	ppm
Timer base clock 2	fclk2		32.768		kHz
Timer base clock 2 accuracy				+/-20	ppm
Timer base clock 2 aging				+/-3	ppm/year
Real Time Clock base clock	fclk		32.768		kHz
Real Time Clock accuracy (25°C)				+/-20	ppm
Real Time Clock temperature coefficient				-0.04	ppm/(°C)²
Real Time Clock aging				+/-3	ppm/year

Tab. 52 General Switching Characteristics

7.2. EMI / EMC Specification

7.2.1. Relevant Standards

The IPC/NETIPC-6 has been designed to comply the the following standards:

- EN 55022 Information technology equipment-
  Radio disturbance characteristics-
  Limits and methods of measurement

- EN 55024 Information technology equipment-
  Immunity characteristics -
  Limits and methods of measurement

- EN 61000-6-2 Electromagnetic compatibility (EMC),
  Part 6-2: Generic standards- Immunity for industrial environments

- EN 61000-6-4 Electromagnetic compatibility (EMC),
  Part 6-4: Generic standards – Emission standard for industrial environments

7.2.2. Emission

The emission tests are still pending. For furhter information please contact the manufacturer.

Test	Limit	Performance Criteria	Result	Remarks
Stationary interference voltage on the AC voltage terminals V-Network 0.15 – 30 MHz Power supply line Control and singal lines	EN 55022	Class A	pending	Compliant with EN 50121-3-2 (referring to EN 55011)
Radiated E-Field, horizontal and vertical polarized E-Field-Anenna 30 – 100 MHz EUT with all cables	EN 55022	Class A	pending	Compliant with EN 50121-3-2 (referring to EN 55011)

Tab. 53 Electromagnetic Emission

7.2.3. Immunity

The immunity tests are pending. For furhter information please contact the manufacturer.

Test	Standard Test level	Perfromance Criteria	Result	Remarks
Electrostatic discharge (ESD) - indirect on coupling plane with contact discharge - direct on case with air and contact discharge EUT with all cables	EN 61000-4-2 6kV Cont. 8kV Air (metal case)	 B B	 pending pending	Compliant with EN 50121-3-2
Radiated electromagentic field 80 – 1000 MHz, 80% AM (1kHz) EUT with all cables	EN 61000-4-3 20V/m	 A	 pending	Compliant with EN 50121-3-2
Radiated electromagentic field 1.4 – 2.0 GHz, 80% AM (1kHz) 2.0 – 2.7 GHz, 80% AM (1kHz) EUT with connection cable	EN 50121-3-2 10V/m 5V/m	 A A	 pending pending	
Fast transients (EFT) Common Mode, 5/50ns, repetion freq. 5kHz Controll and signal lines Power supply	EN 61000-4-4 2kV 2kV	 B B	 pending pending	Compliant with EN 50121-3-2
Slow transients (Surges) Pulse form 1.2/50us Power supply All other signal lines (L>30m)	EN 61000-4-5 2.0kV (ground) 1.0kV	 B	 pending	Compliant with EN 50121-3-2
Conducted radio frequency 150kHz – 80MHz, 1kHz 80% AM Control and signal lines (L > 3m) Power supply	EN 61000-4-6 10V 10V	 A A	 pending pending	Compliant with EN 50121-3-2

Tab. 54 Electromagnetic Immunity

7.3. Environmental Specification

The IPC/COMPACT6 has been designed to meet the the following standards:

- EN 60068-2-27 Basic environmental testing procedures – Part 2-27:
  Test Ea and guidance: Shock

- EN 60068-2-6 Environmental testing – Part 2-6:
  Test Fc: Vibration (sinusoidal)

7.4. Mechanical Data

The enclosure can house a complete industrial control system with many basic functions. The enclosure with its internal electronic system meets EMI/RFI electromagnetic standards according to the European ”CE”- requirements (see paragraph 1.5). The figure below shows the IPC/COMPCACT6-ML from its three sides.

Label	X [mm]	Y [mm]	D [mm]	Label	X [mm]	Y [mm]	D [mm]
A1	26.31	13.85	DSUB9	A12	222.06	11.12	18 x 10
A2	54.56	15.75	14.5 x 15.5	A13	22.02	34.9	11.2x70.4
A3	71.56	15.75	14.5 x 15.5	A14	7.76	33.05	d3/d4.8x90
A4	91.06	14.35	14.5 x 17	A15	106.68	33.05	d3/d4.8x90
A5	114.06	14.35	14.5 x 17	A16	147.06	29.88	DSUB9
A6	126.56	10.46	d3.5	A17	181.06	29.88	DSUB9
A7	147.06	14	DSUB9	A18	58.54	14	DSUB9
A8	181.06	14	DSUB9	A19	92.54	14	DSUB9
A9	200.56	9.38	d2.3	A20	58.54	29.88	DSUB9
A10	200.56	12.68	d2.3	A21	92.54	29.88	DSUB9
A11	200.56	15.98	d2.3				

Tab. 55 Coordinates

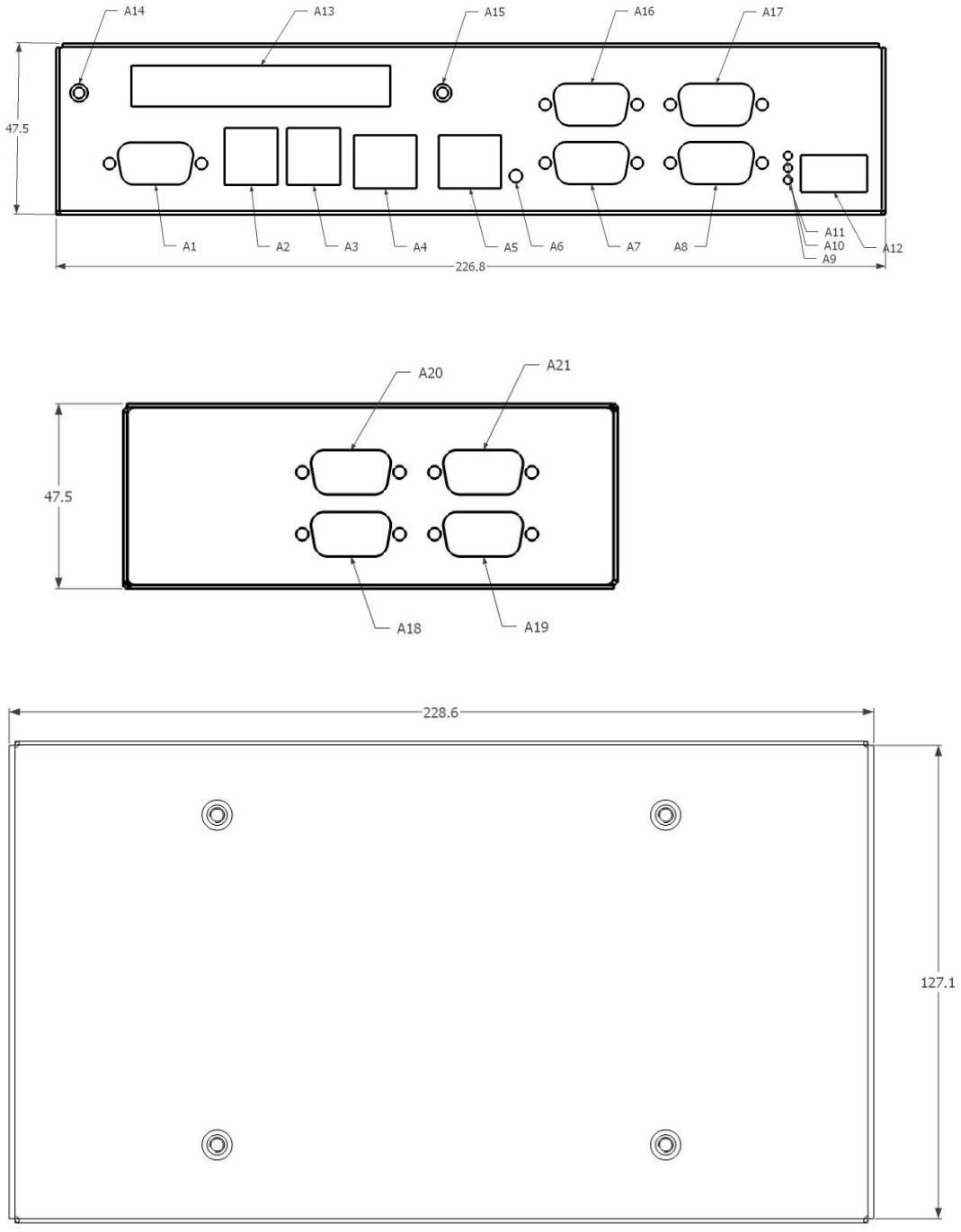

Fig. 48 Three side view of the IPC/COMPACT6-ML enclosure (front, side, bottom)

8 Firmware

8.1. Software Structure

The x86 CPU board based PC/104 system is based on the following software structure:

BIOS (Basic Input/Output System)

- Power On Self Test (POST)
- Initialization of standard peripheral devices
- Boot procedure for the Operating System

  Note : Refer to the BIOS documentation for detailled information

OS (Operating System)

- Initialization of additional peripheral devices
- Start procedure for the Application Programs

  Note : Refer to the OS documentation for detailled information

Application Programs

- Initialization of NETSBC-6A system, communications and external devices
- Start procedure for the Control Tasks

  Note : Refer to the Application Programs documentation for detailled information

8.2. Firmware Functions

The NETSBC-6AC board is setup with the firmware IPC/NETIPCFW-6A (see documentation DOC/NETIPCFW6 for details). Some standard PC/AT peripheral devices (e.g. VGA, Keyboard/Mouse, Serial Ports, IDE interface) are directly supported by the BIOS, BIOS extensions and Operating Systems. Some peripheral devices are directly supported by standard communication software (e.g. TCP/IP stacks, TCP packet drivers) others need special programming according to the freely available sample software IPC/IOCOMSW6-1A (e.g. Watchdog). Please refer to the appropriate documentation for detailed information.

8.3. Application Programming Interface (API)

The NETSBC-6AC board does not contain any special API besides the installed BIOS and DOS. Refer to the BIOS and Operating System documentation (included in DOC/NETIPCFW6) for API specifications.

8.4. Operating Systems

Syslogic offers an implementation for the following operting systems (OS):

Debian Linux Distribution
IPC/DEBIAN-40A

Microsoft Windows CE 5.0 and CE6.0
IPC/WINCE-50A
IPC/WINCE-60A

Microsoft Windows XP Embedded
IPC/WINXPE-6A

Others on request.

Important Note

When implementing a BSP for a new OS be sure to use the “Pentium Platform”.

9 Product Revision History

9.1. Hardware

This paragraph lists the different hardware revisions of the NETSBC-6AC boards delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	Product Revision	Logic Revision ID Register	Remarks
IPC/COMPACT6-2A	#1		Original Release, RoHS compliant
IPC/NETSBC-6A2	#1	03h	Original Release, RoHS compliant
IPC/COMPACT6-2A	#2		Power fail and shutdown issue solved, RoHS compliant
IPC/NETSBC-6A2	#2	03h	Power fail and shutdown issue solved, RoHS compliant
IPC/COMPACT6-2A	#3		DVI interface instead of VGA
IPC/NETSBC-6A2	#3		
IPC/COMPACT6-2A	#4		Power Management added
IPC/NETSBC-6A2	#4		Power Management Controller added
IPC/COMPACT6-2A	#4.1		Several issue solved
IPC/NETSBC-6A2	#4.3	06h 01h	Several issue solved
IPC/COMPACT6-2AC	#1		Original Release, RoHS compliant
IPC/NETSBC-6AC	#1	03h 01h	Original Release, RoHS compliant additional Logic Revision ID
IPC/COMPACT6-2AC	#2		Power fail and shutdown issue solved, RoHS compliant
IPC/NETSBC-6AC	#2	03h 01h	Power fail and shutdown issue solved, RoHS compliant
IPC/COMPACT6-2AC	#3		DVI interface instead of VGA
IPC/NETSBC-6AC	#3		
IPC/COMPACT6-2AC	#4		Power Management added
IPC/NETSBC-6AC	#4		Power Management Controller added
IPC/COMPACT6-2AC	#4.1		Several issue solved
IPC/NETSBC-6AC	#4.3	06h 01h	Several issue solved

Tab. 56 Hardware Revision State

9.2. Firmware

Please refer to the firmware documentation DOC/NETIPCFW6 for detailed information.

Important Note

This document always covers the latest product revision listed in Tab. 56.
Please contact the manufacturers technical support for upgrade options.

10 Manufacturer Information

10.1. Contact

Our distributors and system integrators will gladly give you any information about our products and their use. If you want to contact the manufacturer directly, please send a fax or email message containing a short description of your application and your request to the following address or use one of the information or technical support request forms on our internet homepage:

Syslogic Datentechnik AG
Täfernstrasse 28
CH-5405 Baden-Dättwil / Switzerland

Email: info@syslogic.com
www: http://www.syslogic.com
Phone +41 (0)56 200 90 40
Fax: +41 (0)56 200 90 50

Technical support:
support@syslogic.com